

KyloRen 13" Schematics

KabyLake-R


2017-06-29

REV : -1

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DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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Title

Cover Page

Size
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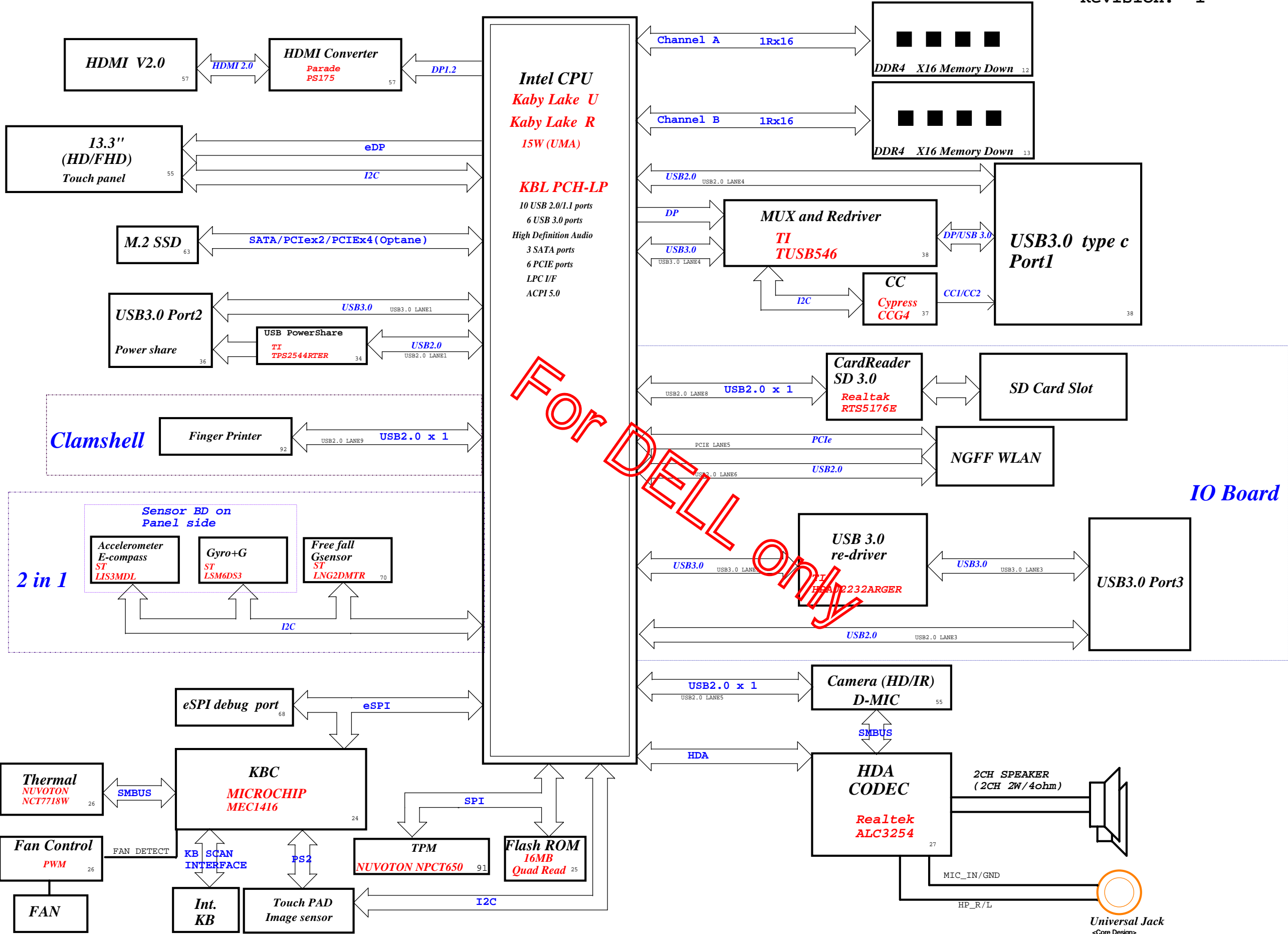
Rev
A00

Date: Thursday, June 29, 2017

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KBL-U(R) 13" CPU 15W Block Diagram

Project code: 4PD0B5010001
PCB P/N: 16839
Revision: -1



Universal Jack
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DDR4 ball type: Non-Interleaved Type

Figure 4-40. KBL U DDR4 x8 Memory Down Placement and Block Diagram

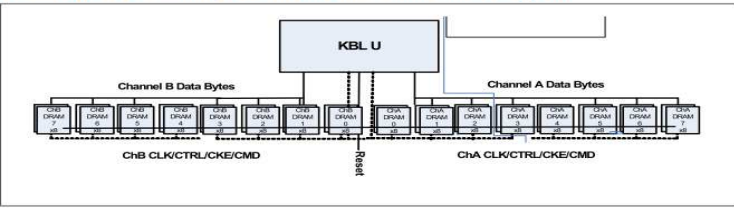
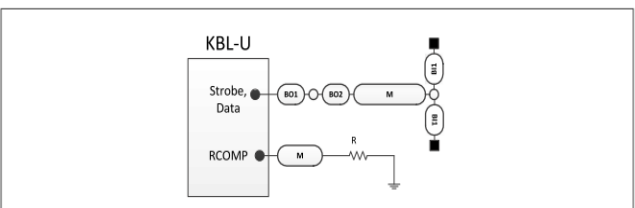


Figure 4-42. KBL U DDR4 x8 Memory Down DQ/DQS/RCOMP Signals

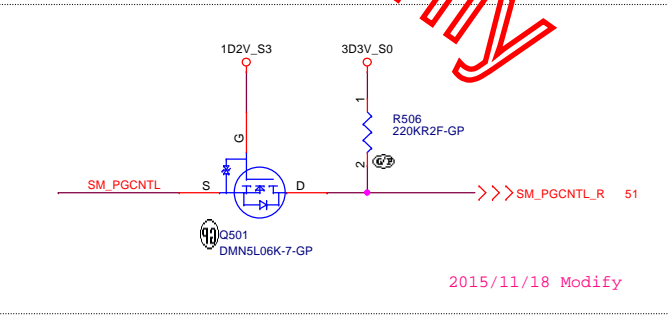


DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

Table 4-48. ODT Signals Connectivity Table (Sheet 2 of 2)

Processor	Memory type	Side	Signal	Rule	Notes
KBL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR3L Memory Down	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
DDR3L SODIMM	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DIMMs' ODT[0]. Processor's ODT[1] connected to DIMMs' ODT[1].	1,3
		DIMMs	ODT[1:0]		
DDR3L Mixed Memory Down and SODIMM	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
DDR4 Memory Down	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	1,3
		DRAMs	ODT[1:0]		
DDR4 SODIMM	Processor	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] balls connected to DIMM ODT[1:0] balls.	1,3
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - KBL-Y LPDDR3, RVP5 - KBL-U LPDDR3, RVP7 - KBL-U DDR3L SODIMM).
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT_NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT_WR (set by BIOS after power training). Otherwise ODT gets RTT_NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2R x8 dual side.



Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

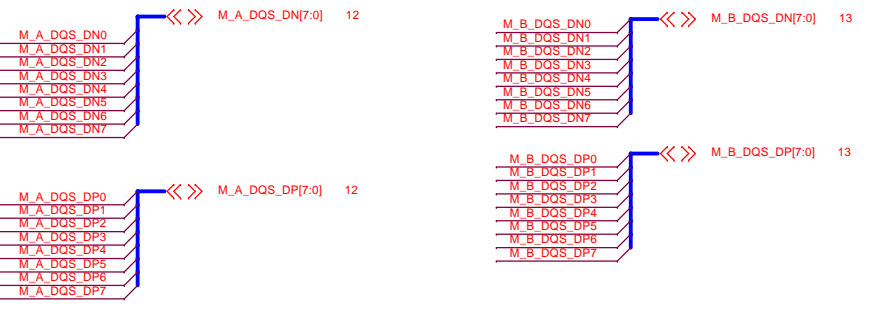
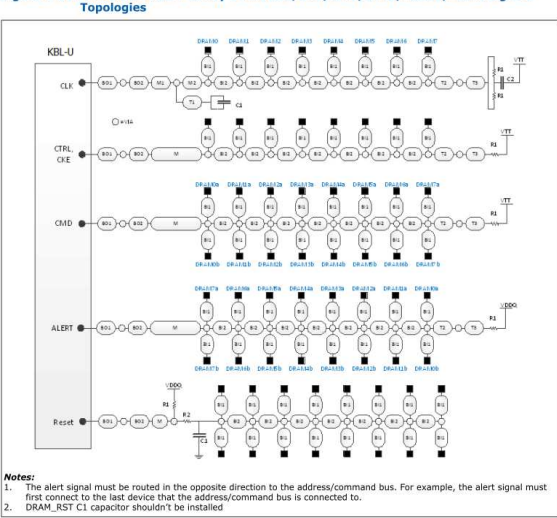
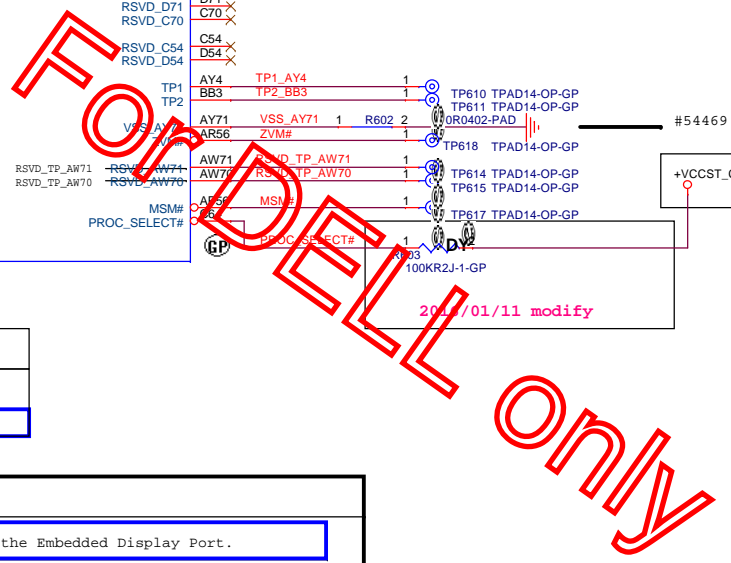


Figure 4-41. KBL U DDR4 x8 Memory Down CLK/CKE/CMD/CTRL/ALERT/Reset Signals Topologies

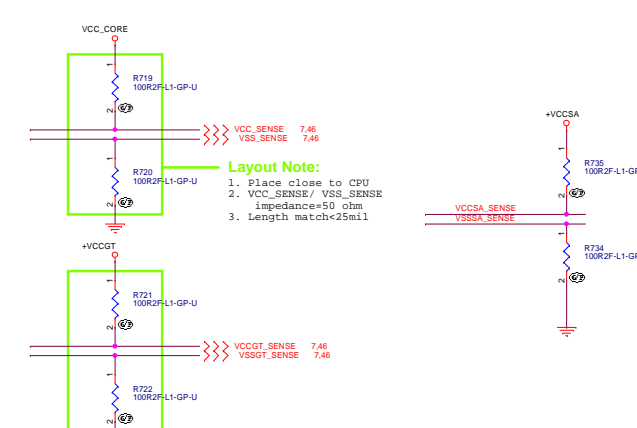
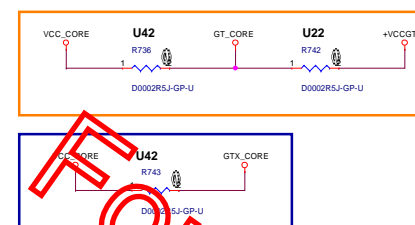
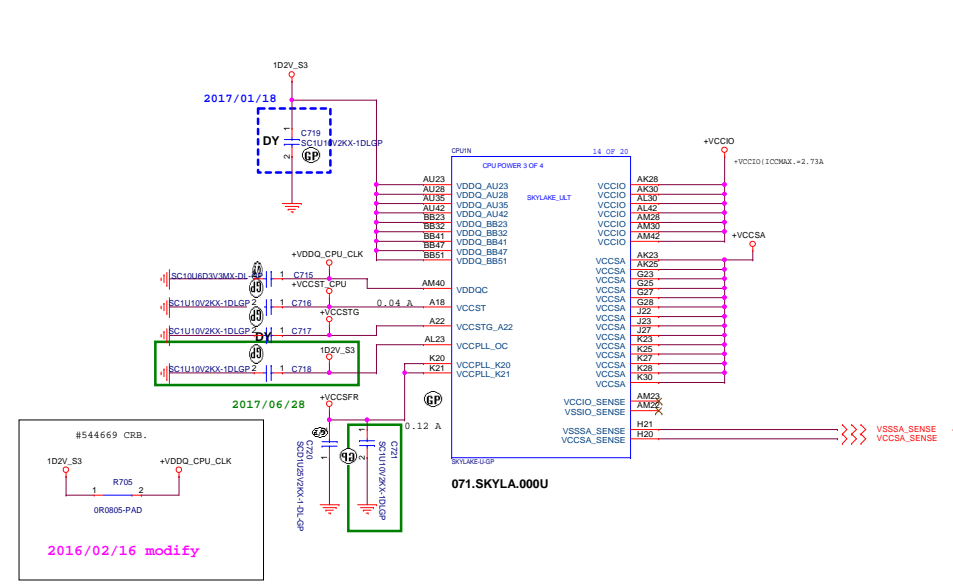
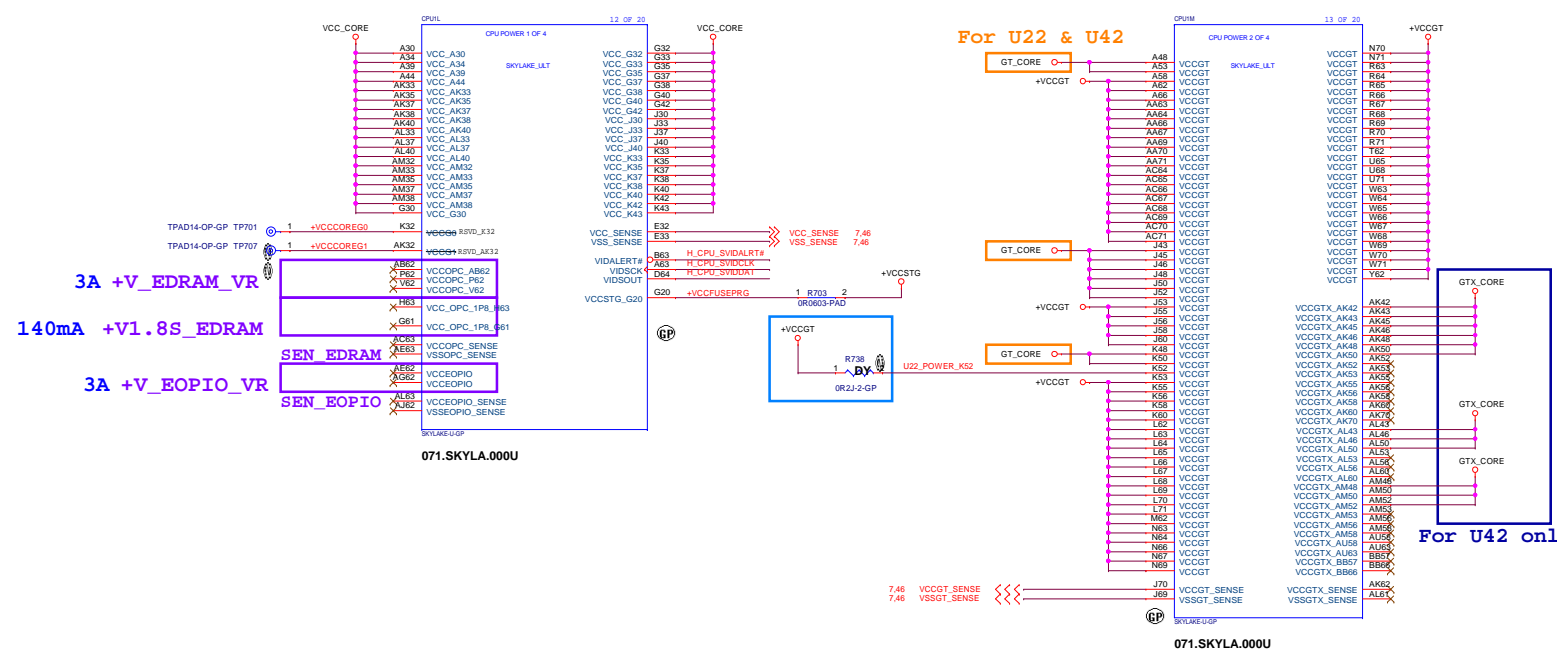


Notes:
1. The alert signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.
2. DRAM_RST C1 capacitor shouldn't be installed

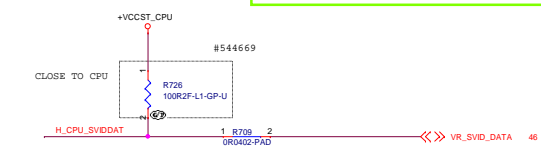


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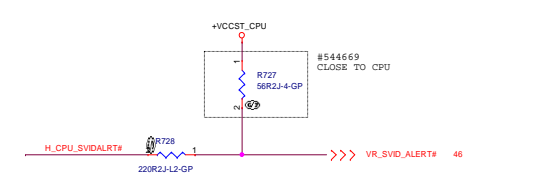
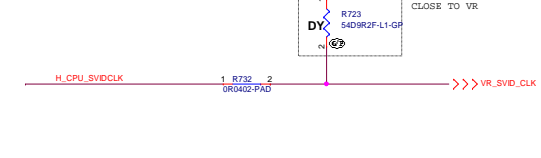




SVID DATA



SVID CLOCK



SVID_543016

Figure 10-7. Routing Illustration for SVID Topology

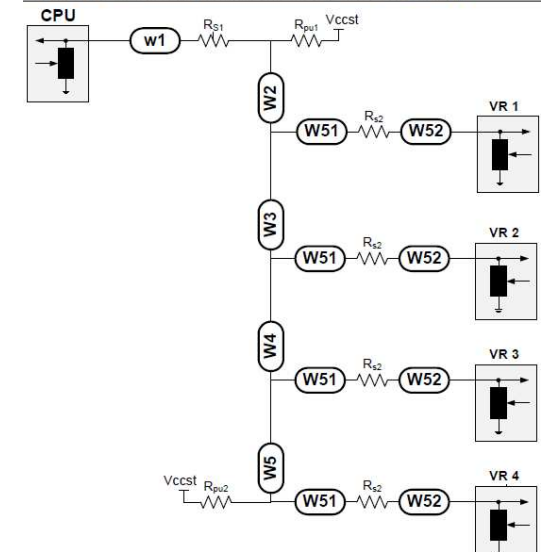
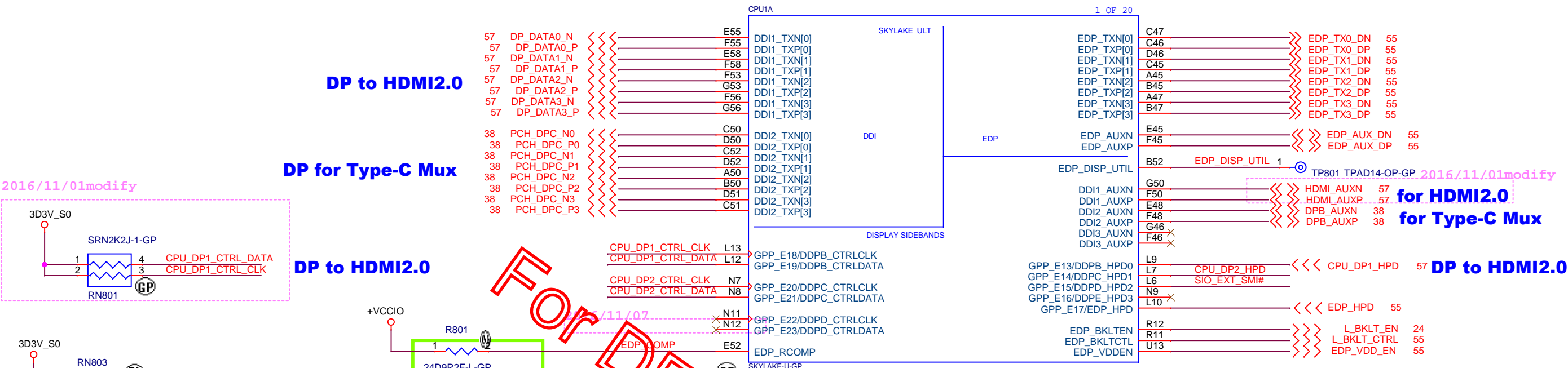


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{pu1} [Ω]	R _{pu2} [Ω]	R _{s1} [Ω]	R _{s2} [Ω]	VCC _{GT} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT#							56	Empty	220	0	

SSID = CPU



2016/11/01modify

DP for Type-C Mux

DP to HDMI2.0

2016/11/07

2016/11/07
Touch_panel_Resort_remove

2016/11/01modify

for HDMI2.0

for Type-C Mux

DP to HDMI2.0

2016/12/28 DP for Type-C Mux

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils


(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 \pm 1% Ω resistor.

071.SKYLA.000U
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

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CPU (DISPLAY)

Size A3

Document Number

Rev

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A00

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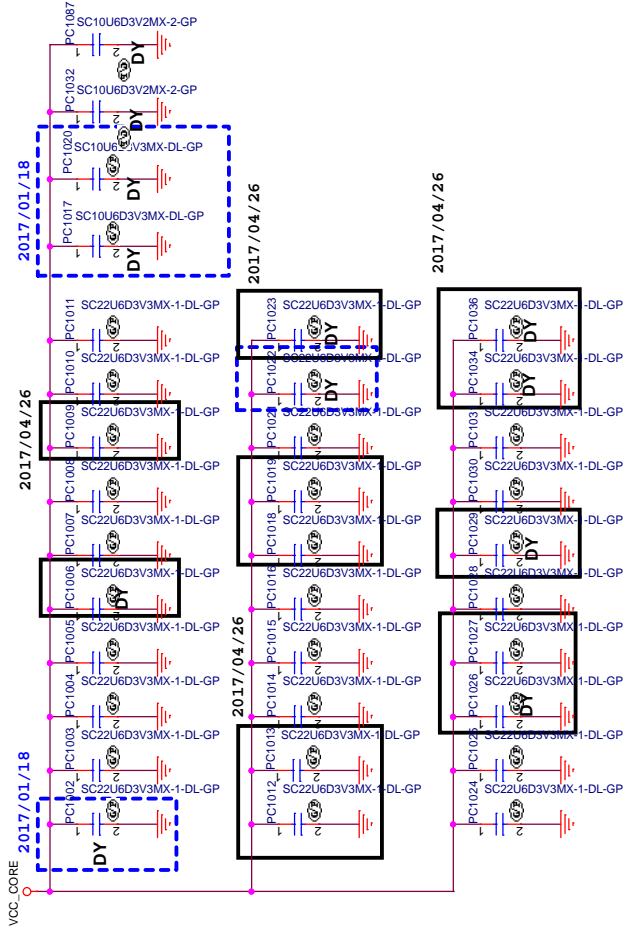
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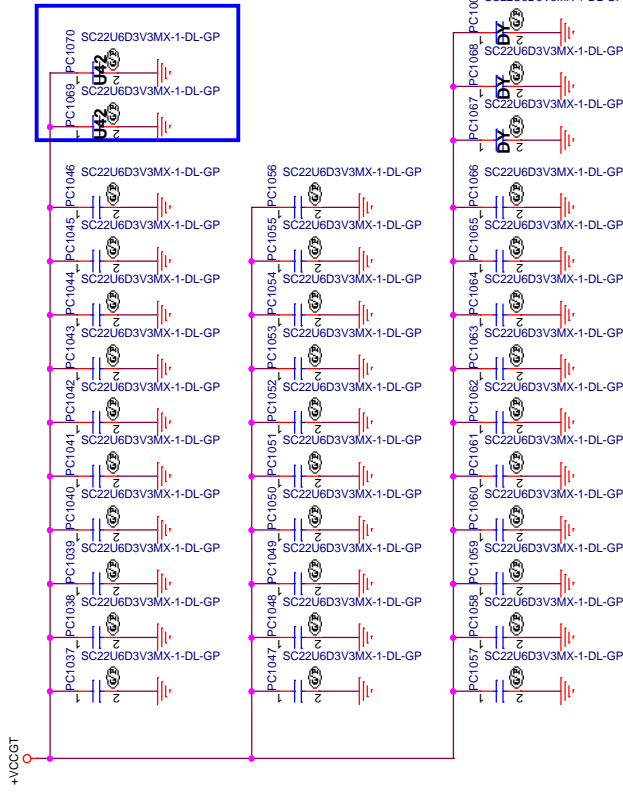
VCC_CORE

U-line 22 15W
IccMax current-10ms max = 31 A
22U 0603 x 30
10U 0402 x 2 (2DY)



VCCGT

U-line 22 15W
IccMax current-10ms max[A] = 64 A
22U 0603 x 30 (3 DY)



VCCSA

22U 0603 x 5 (3DY)

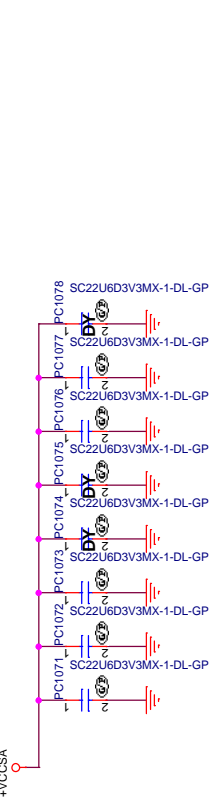


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (@4.5mO ESR) 2x 220uF (@4.5mO ESR)	Placed at backside side near to VR output Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603 7x 10uF 0402 15x 1uF 0201		Place on secondary side, underneath the package
VCCGT	10x 10uF 0402 12x 1uF 0201	8x 47uF 0805 (6.3V) ¹ 8x 10uF 0402	Place as close to the package as possible Place on secondary side, underneath the package
VCCGTx	8x 10uF 0402	3x 47uF 0805 (6.3V) ¹ 7x 22uF 0603 3x 47uF 0805 5x 22uF 0603	Place as close to the package as possible Additional components needed when supporting 23e Place on secondary side, underneath the package Only needed when supporting 23e
VCCSA	7x 10uF 0402 7x 1uF 0201	8x 22uF 0603	Only needed when supporting 23e Place on secondary side, underneath the package
VCCIO	2x 10uF 0402 4x 1uF 0201	6x 10uF 0402	Place as close to the package as possible Place on secondary side, underneath the package
VDDQ	2x 10uF 0402 4x 1uF 0201	4x 1uF 0402	Place as close to the package as possible Place on secondary side, underneath the package
VDDQC	1x 1uF 0201	4x 10uF 0402	Place as close to the package as possible
VCCPLL		1x 1uF 0402	Place on secondary side, underneath the package
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 48-5. Decoupling Requirements for Kaby Lake U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcccore	2x 10 uF 0402		Place on secondary side, underneath the package. Only needed when supporting 23e
Vccgpc	1x 10 uF 0402 6x 1 uF 0201		Place on secondary side, underneath the package. Only needed when supporting 23e
VCC (for 0.55mm Z height Solution Only) (Note 5)	27x 10 uF 0402 35x 1 uF 0201	8x 47 uF 0805 (6.3V) ¹ 8x 10 uF 0402	Place on secondary side, underneath the package Refer to diagram in Note 3 below for placement recommendation of 0201 caps Place as close to the package as possible

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CPU (Power CAP1)

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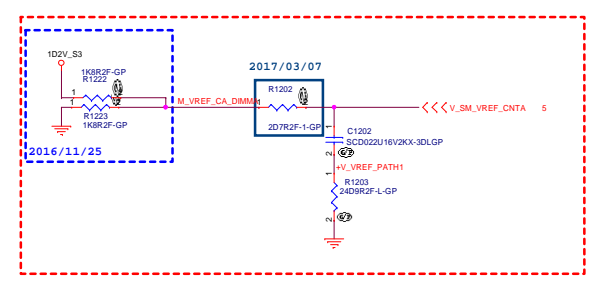
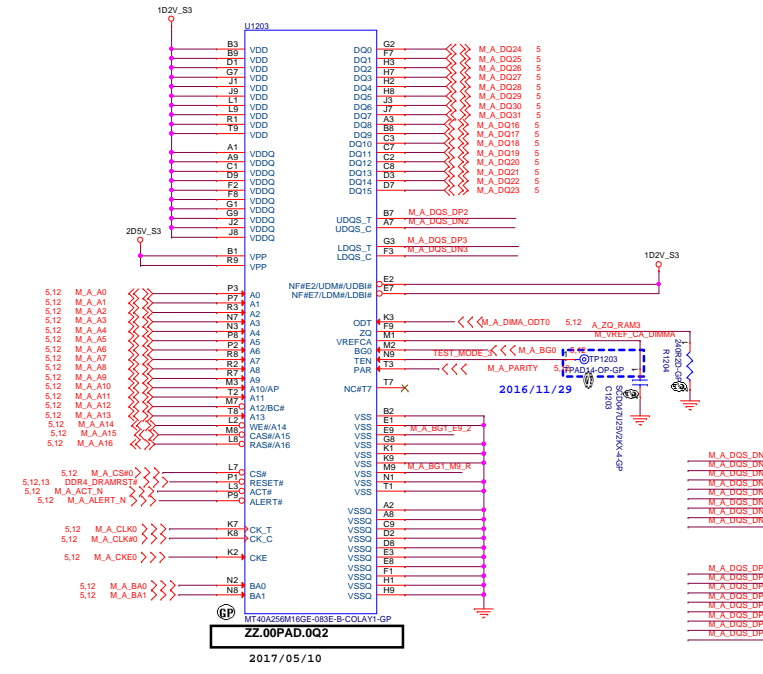
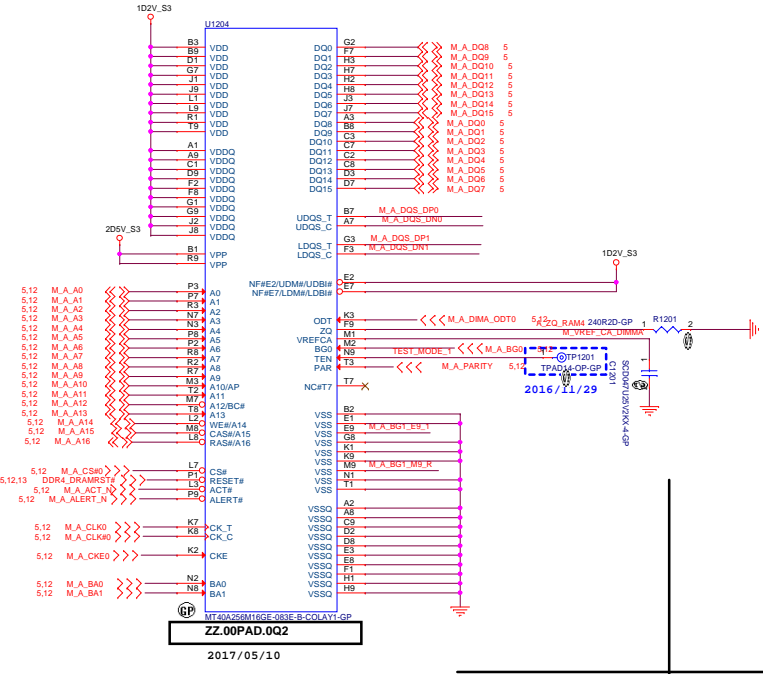
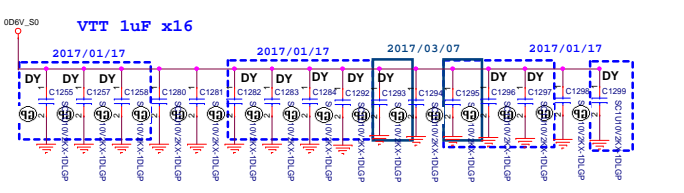
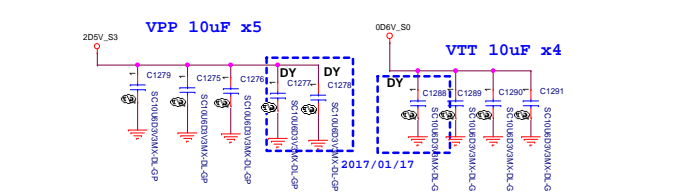
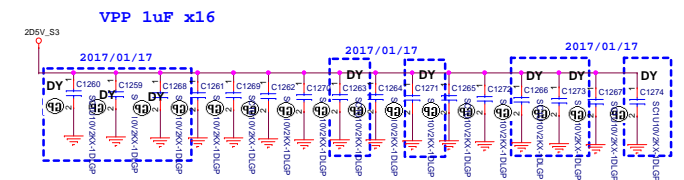
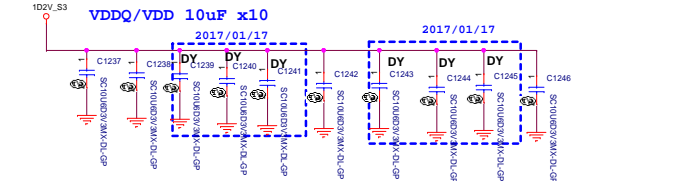
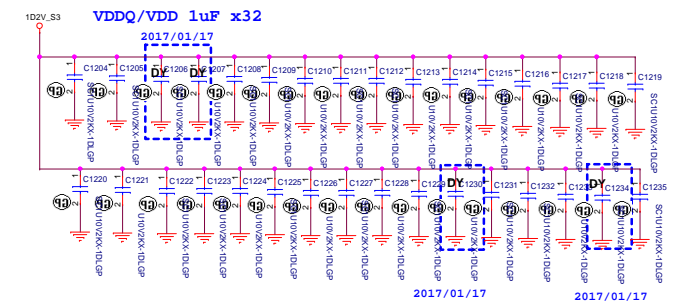
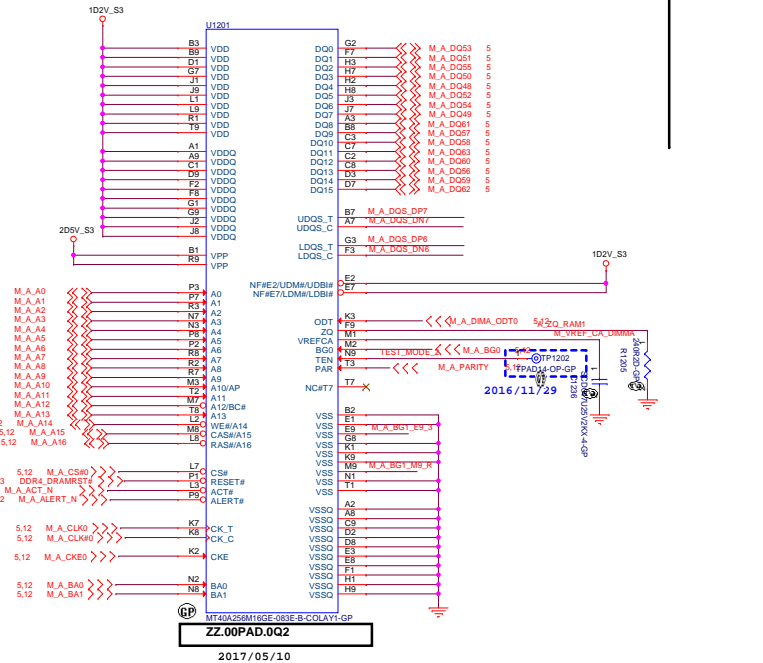
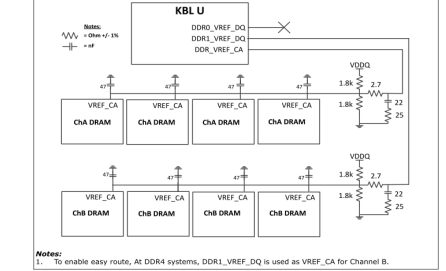


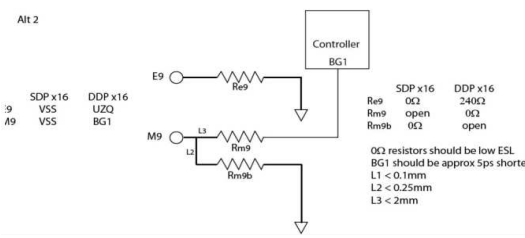
Figure 4-50. KBL U DDR4 x16 Devices Memory Down VREF-CA Overview



SDP & DDP SETTING

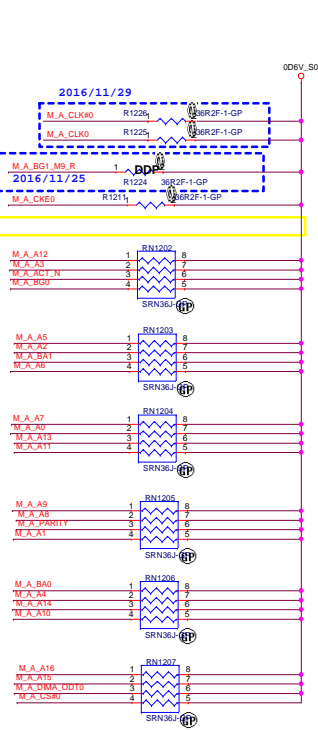
DDP x16 and SDP x16 Compatible Layout

▶ Alternate two layout, risk of VSS offset increases a little



CLK

CTRL/CKE/CMD



ALERT

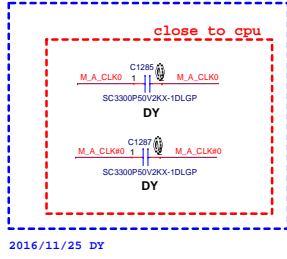
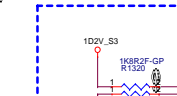
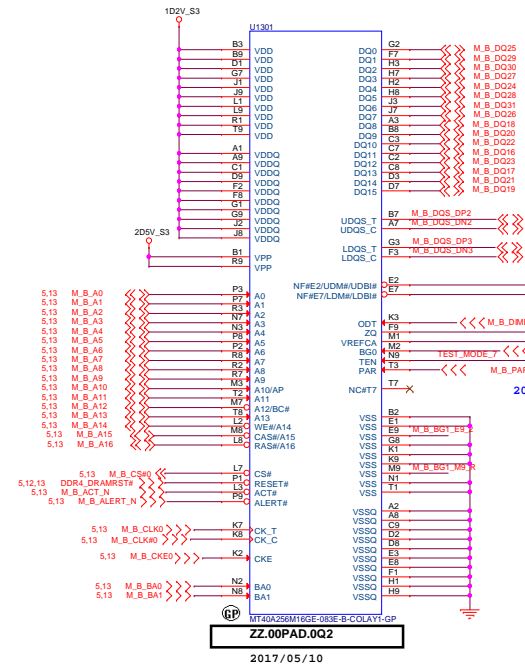
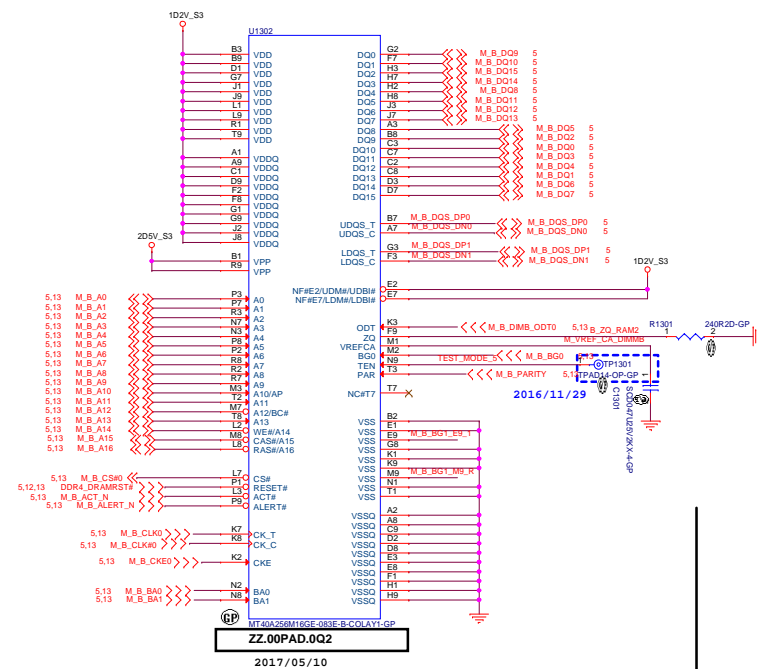


Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

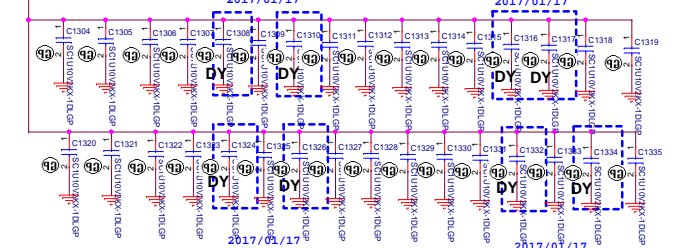
Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 Memory Down x16 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1 μ F (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10 μ F (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1 μ F (0402)	
		Distributed around the DRAM devices	5x 10 μ F (0603)	
VTT		2 as near each x16 DRAM device as possible	16x 1 μ F (0402)	
		Distributed around the DRAM devices	4x 10 μ F (0603)	

Table 4-55. DDR4 Memory Down Power Plane Decoupling (Sheet 2 of 2)

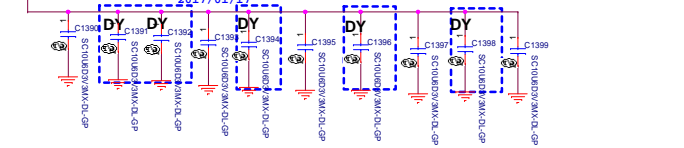
Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 Memory Down x16 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	64x 1 μ F (0402) (All stuffed)	
		Distributed around the DRAM devices	20x 10 μ F (0603) (min of 12 stuffed)	
	VPP	2 as near each x16 DRAM device as possible	32x 1 μ F (0402)	
		Distributed around the DRAM devices	10x 10 μ F (0603)	
VTT		2 as near each x16 DRAM device as possible	32x 1 μ F (0402)	
		Distributed around the DRAM devices	8x 10 μ F (0603)	



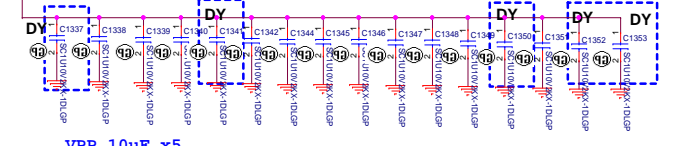
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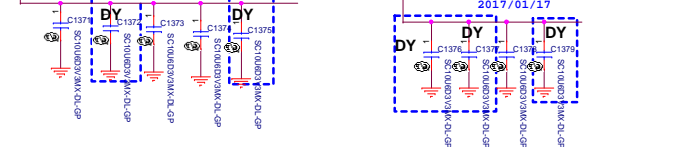
VDDQ/VDD 10uF x10



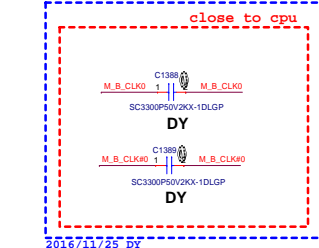
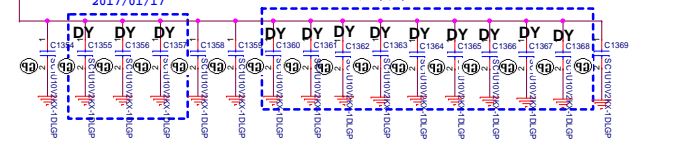
VPP 1uF x16



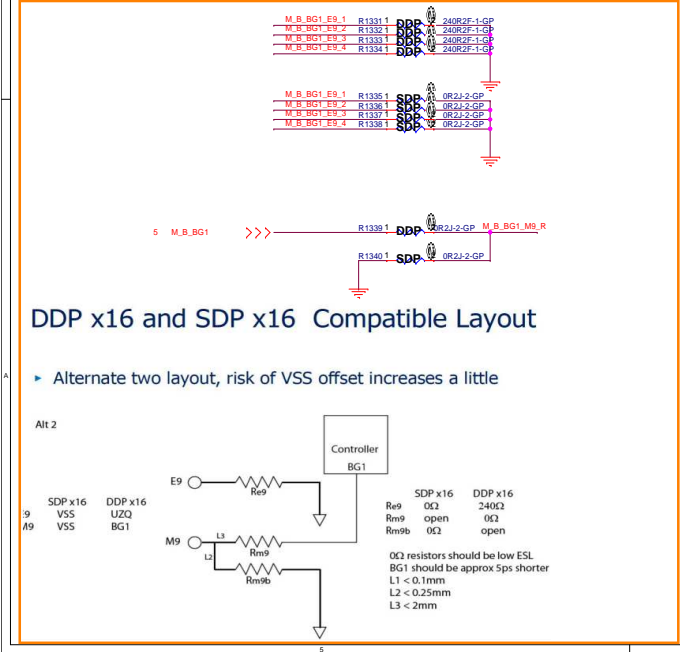
VPP 10uF x5



VTT 1uF x16

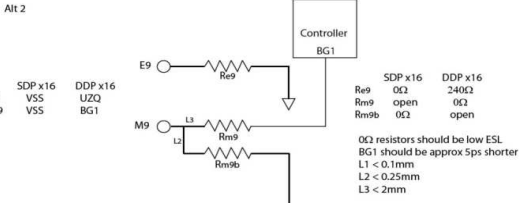


SDP & DDP SETTING



DDP x16 and SDP x16 Compatible Layout

► Alternate two layout, risk of VSS offset increases a little




5	4	3	2	1
D				D
C				C
B				B
A				A

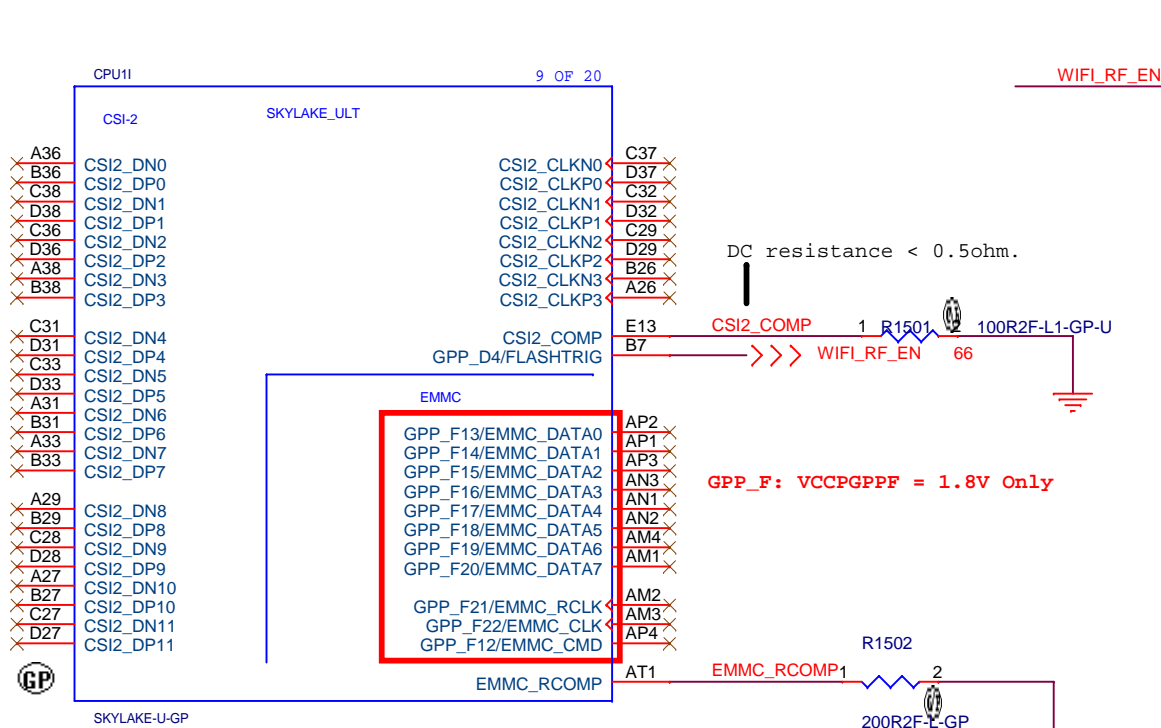
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SSID = PCH



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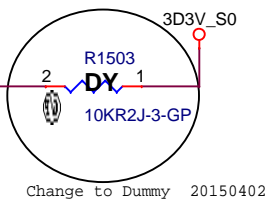


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

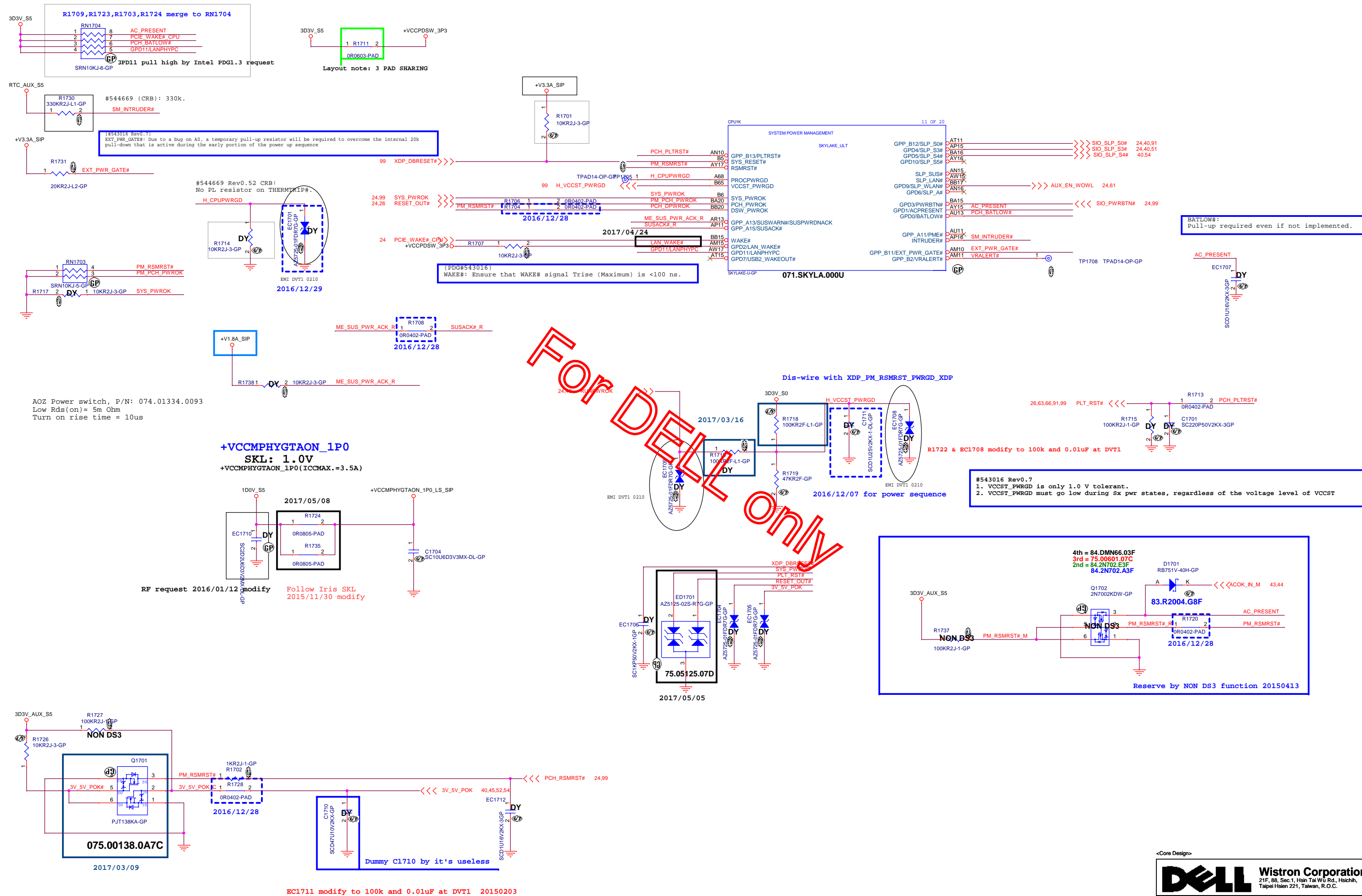
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

For Dell only

<Core Design>

SSID = PCH

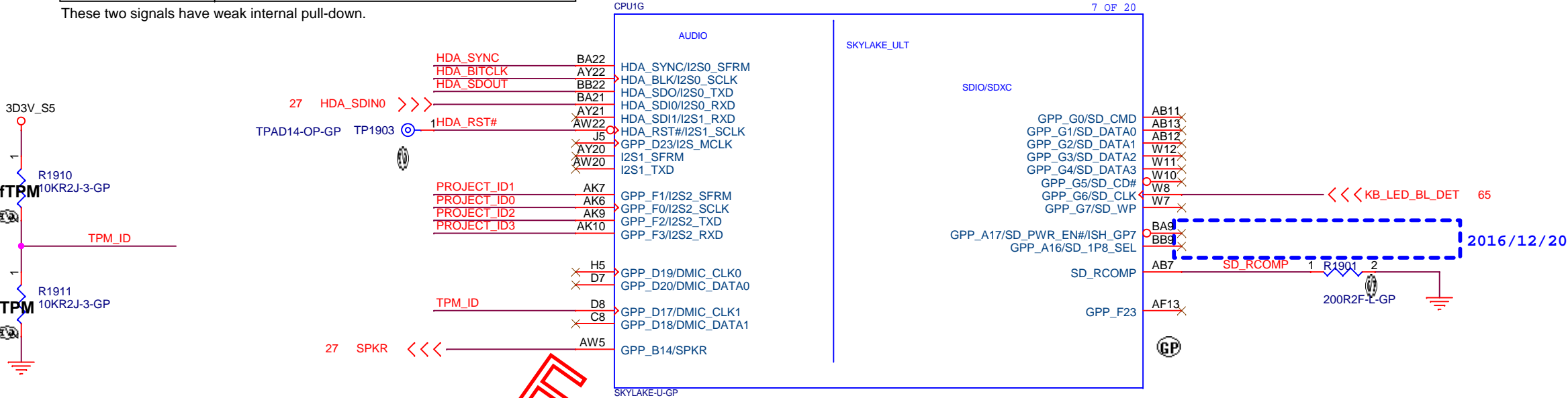


SSID = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

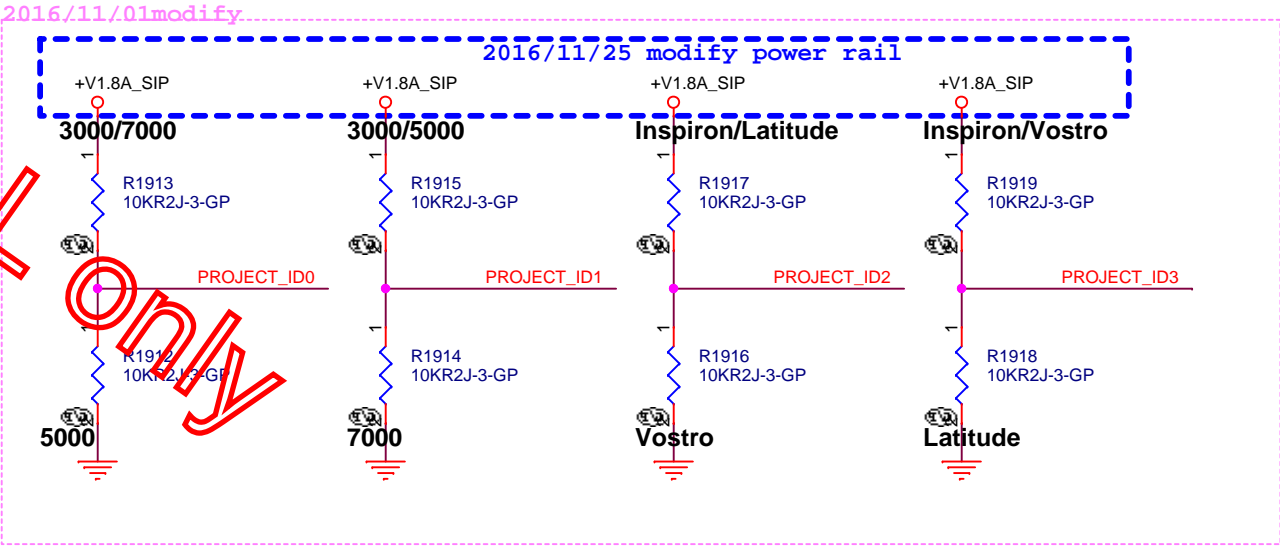
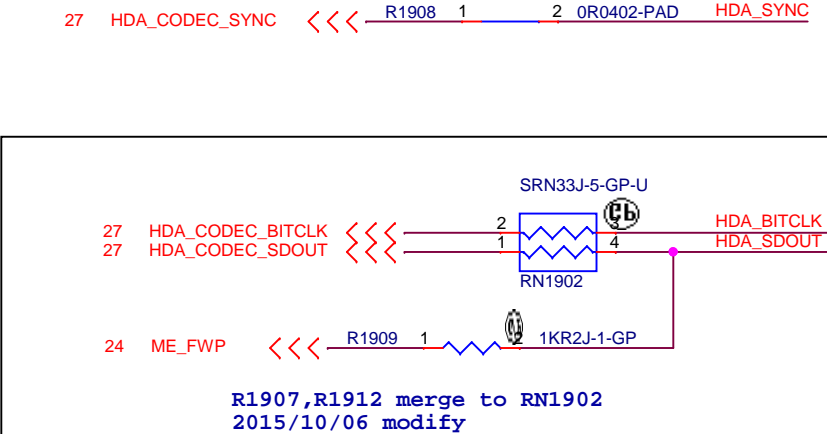
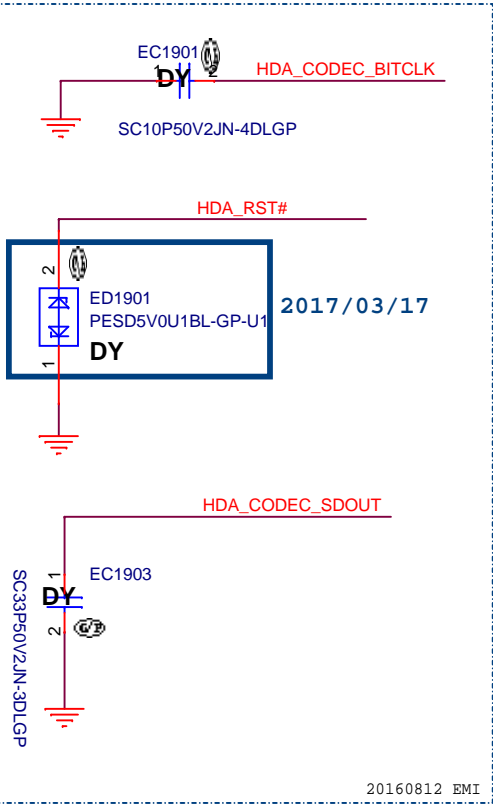
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDO	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

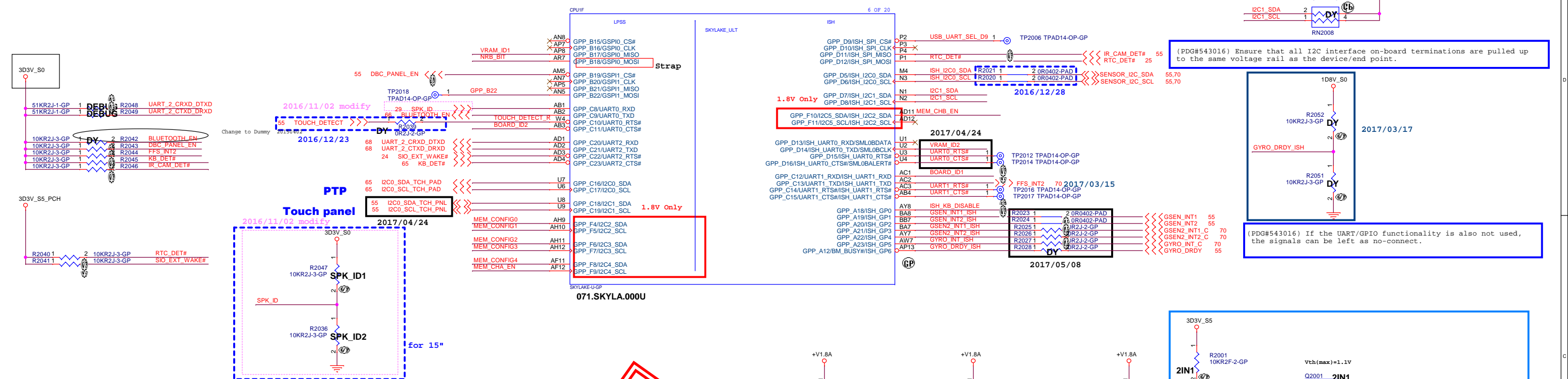
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



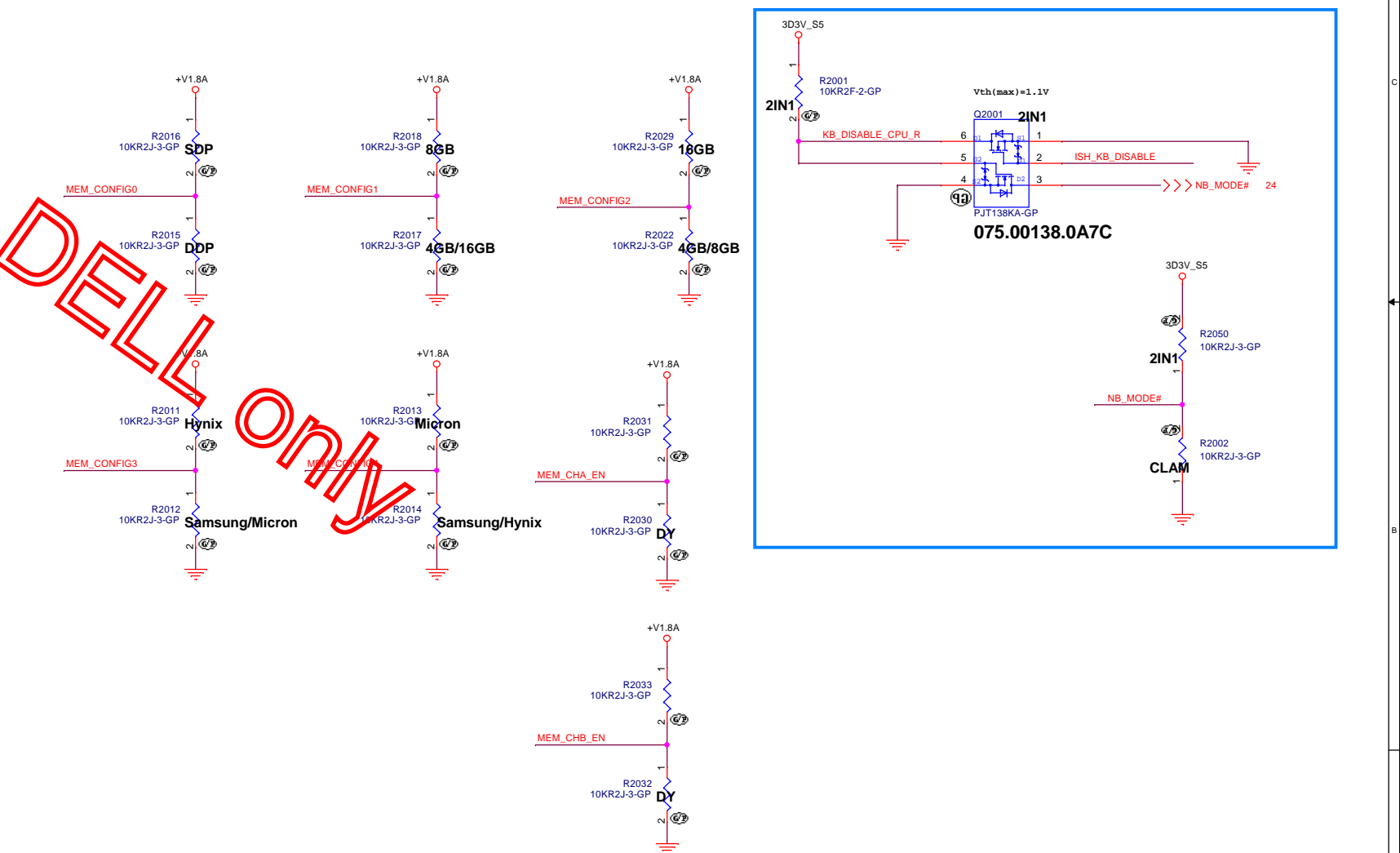
<Core Design>

SSID = PCH



Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron. P/N	Capacity
Samsung	0	01	00	K4AAG165WB-BCRC	TBD	16G
Hynix	0	01	10	H5ANAG6NAMR-UHC	TBD	16G
Micron	0	01	01	MT40A1G16WBU-083E	072.40116.0B0U	16G
Samsung	1	10	00	K4A8G165WB-BCRC	TBD	8G
Hynix	1	10	10	H5AN8G6NAFR-UHC	TBD	8G
Micron	1	10	01	MT40A512M16JY-083E	072.40512.0B0U	8G
Samsung	1	00	00	K4A4G165WE-BCRC	072.44165.0B0U	4G
Hynix	1	00	10	H5AN4G6NBJR-UHC*	TBD	4G
Micron	1	00	01	MT40A256M16GE-083E	072.40256.0A0U	4G

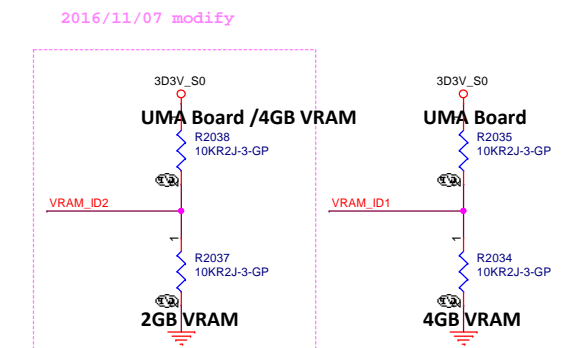
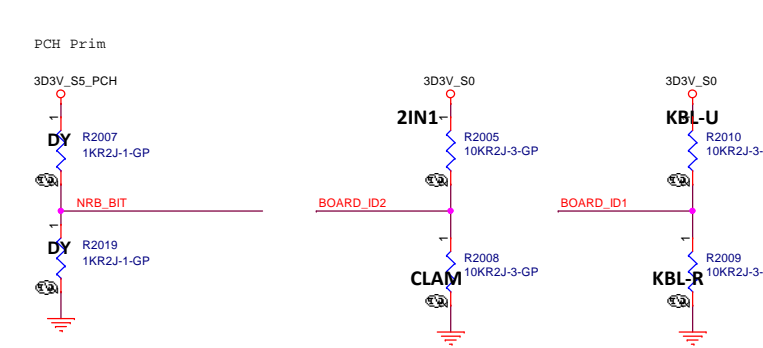
For DELL only

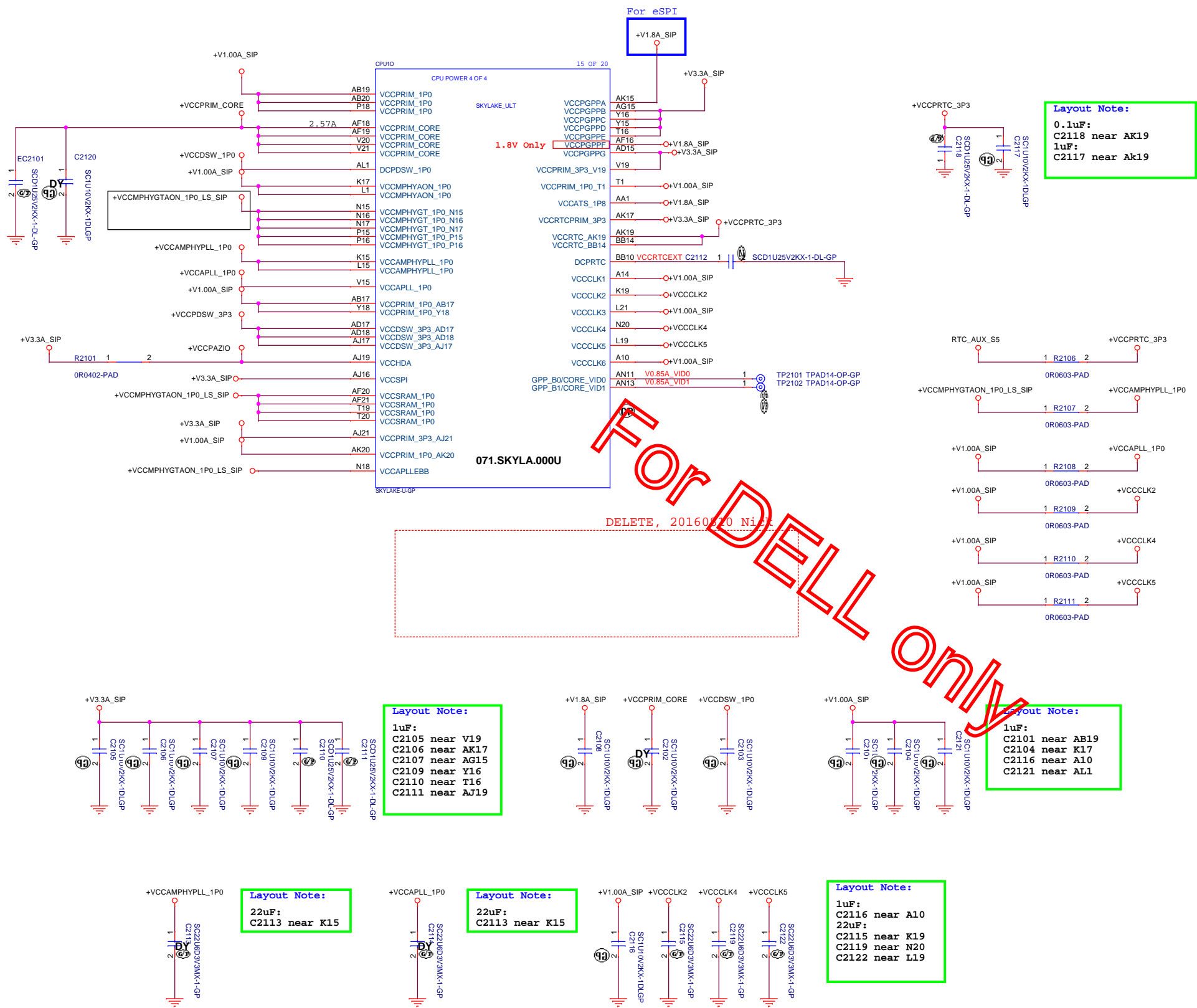


PCH strap pin:

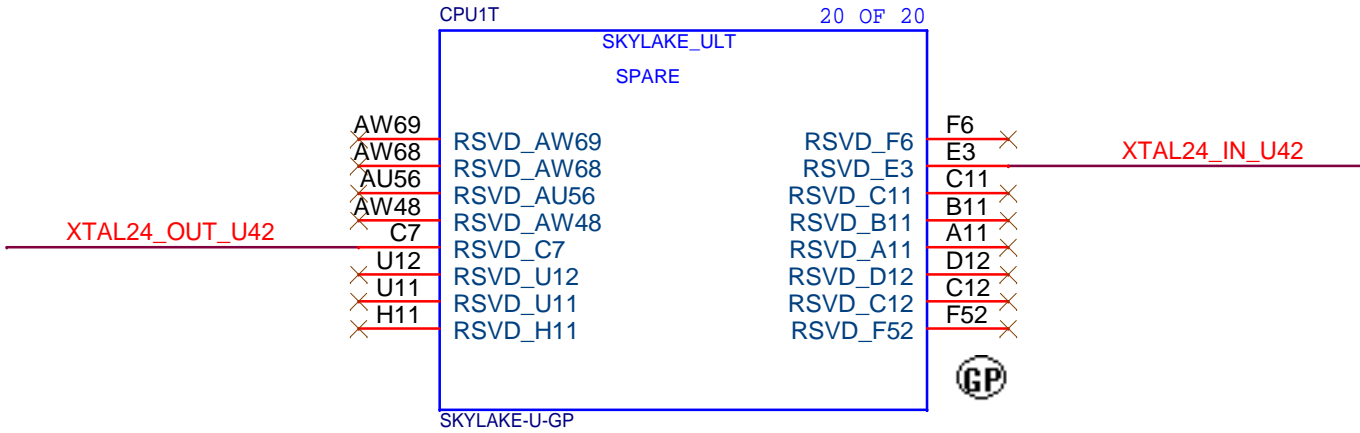
No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

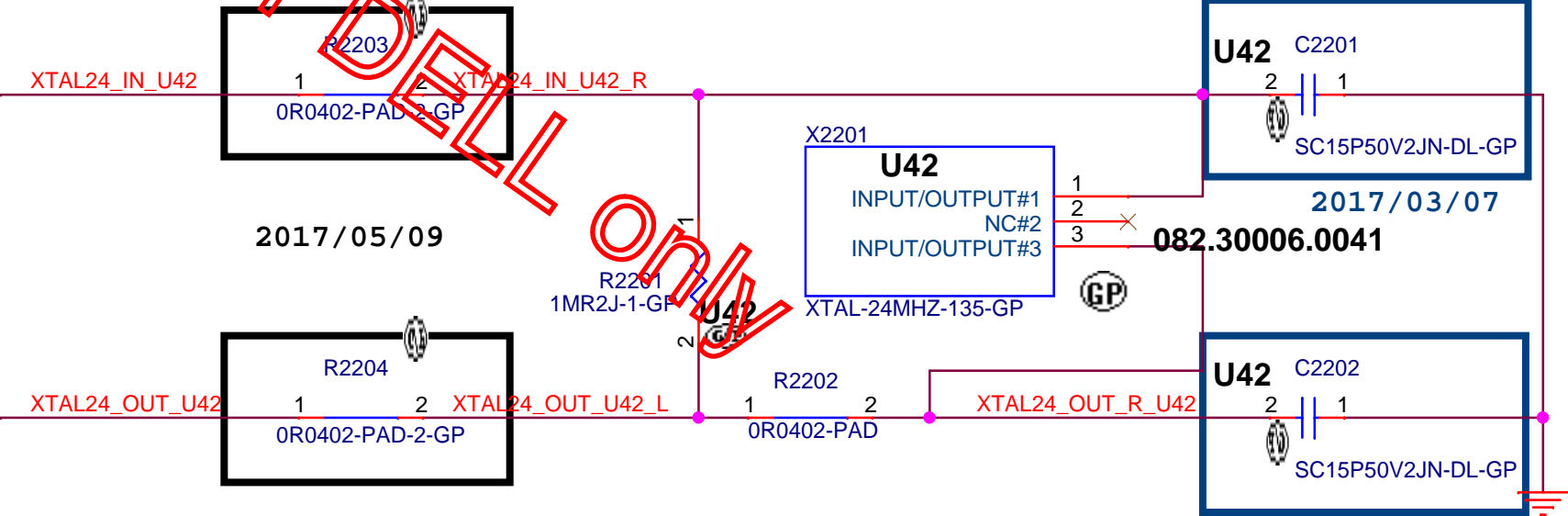





SSID = PCH



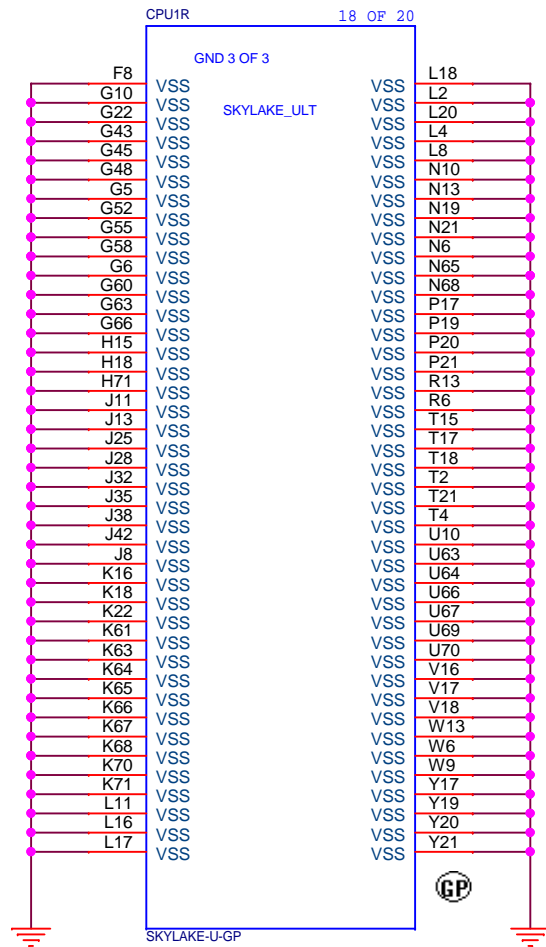
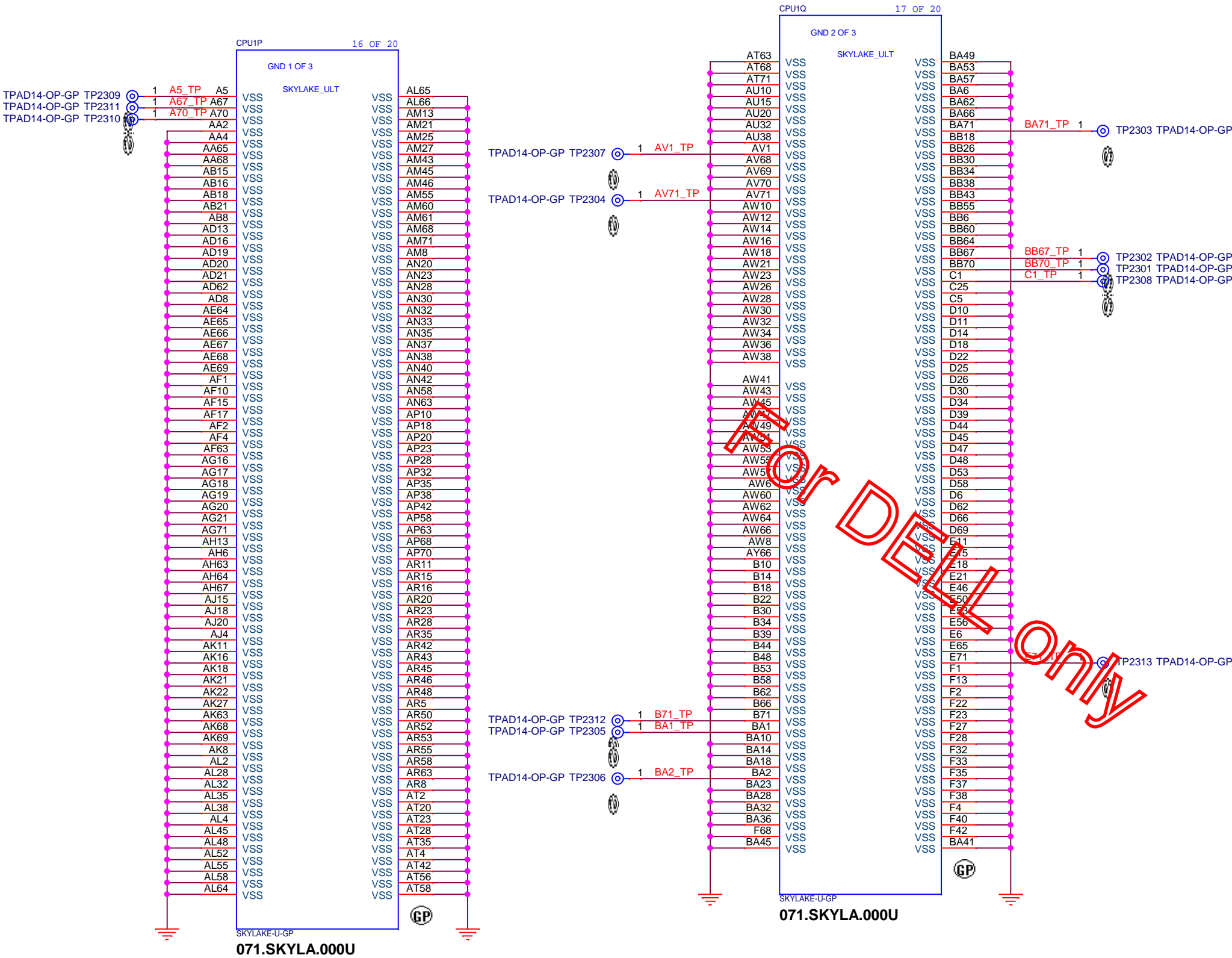
071.SKYLA.000U



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (RSVD)			
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SSID = PCH



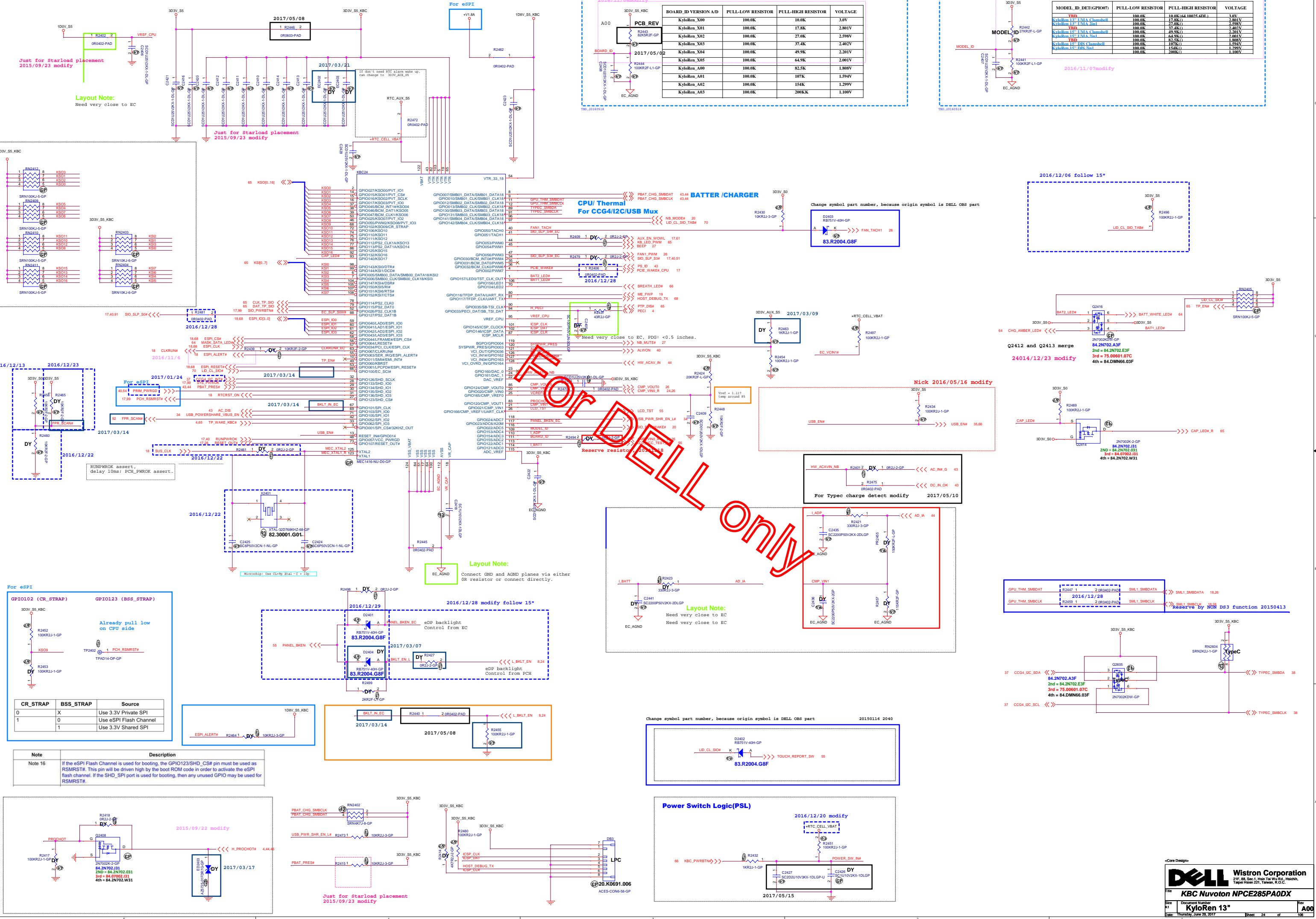
Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	Corner BB1
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner A1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A71
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	Corner A71
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	Corner A71

<Core Design>

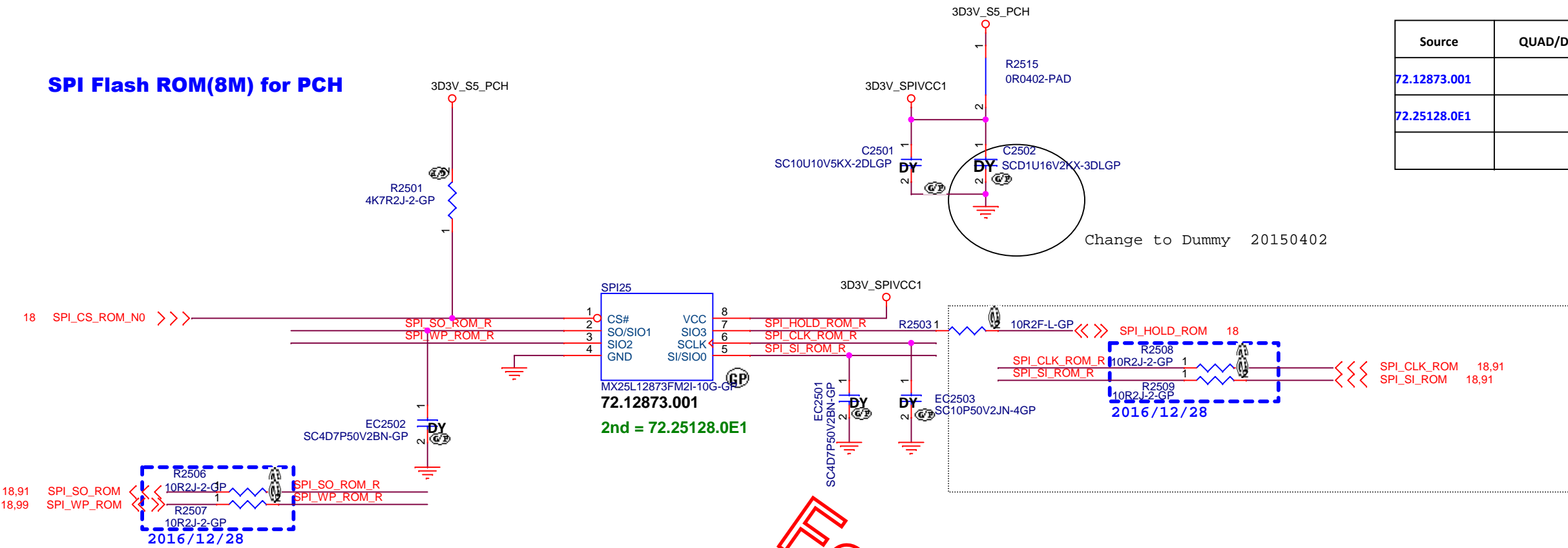


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SSID = SPI Flash

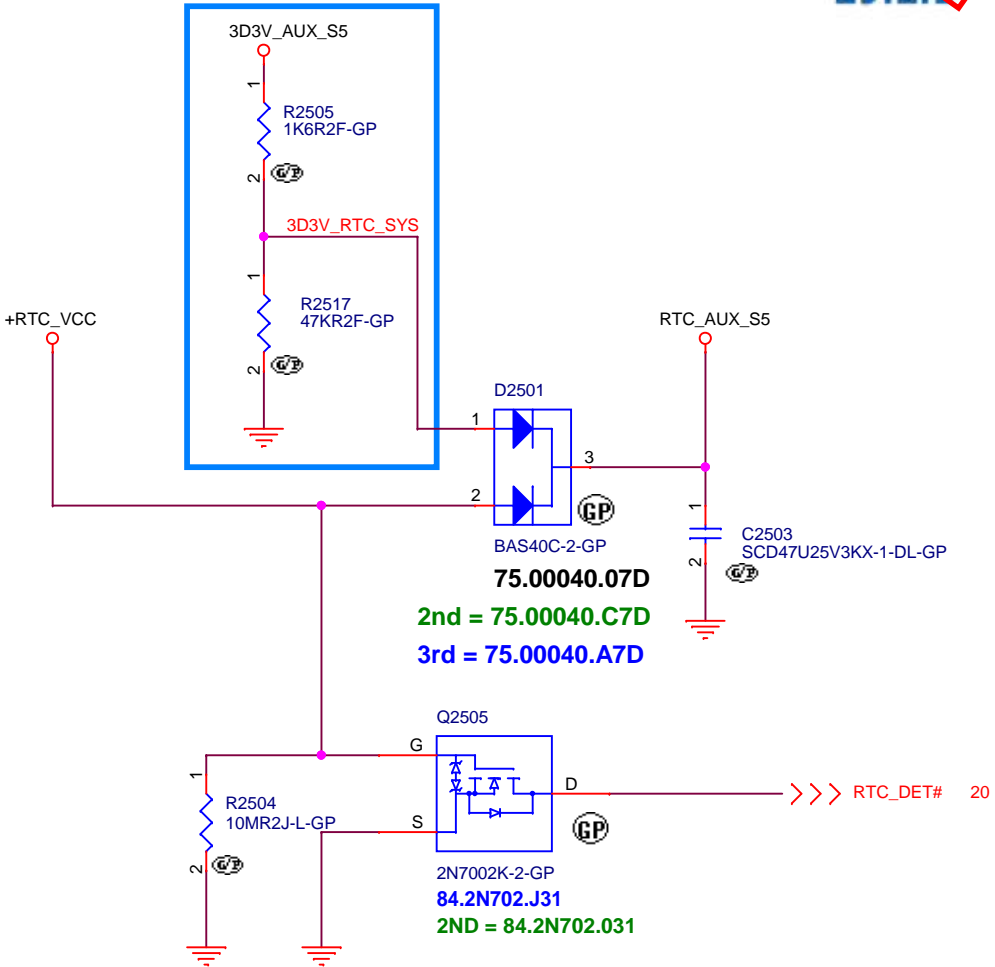
SPI Flash ROM(8M) for PCH



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.12873.001	o	o	o
72.25128.0E1	o	o	o
	o	o	o

Main Func = RTC

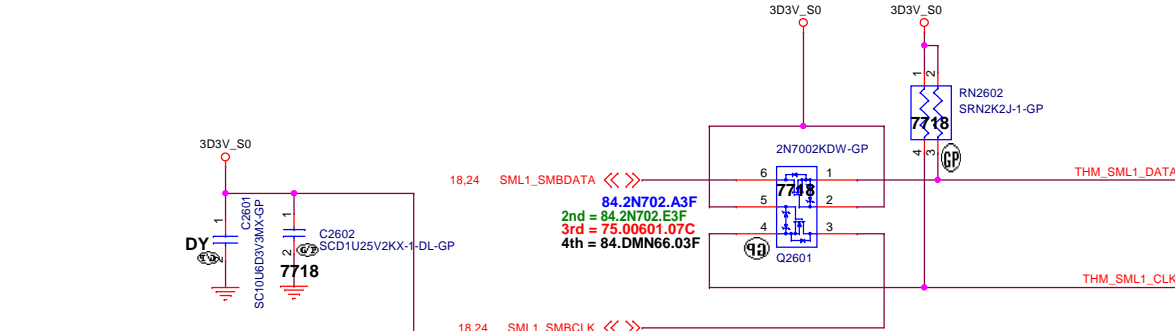
Delivery Voltage 3.19V



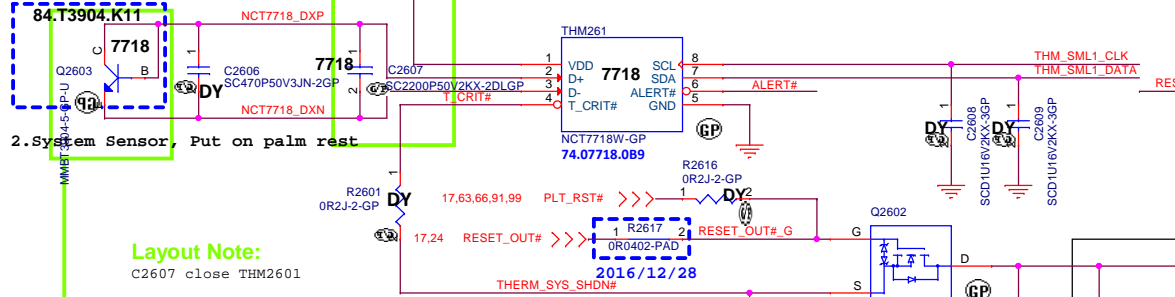
29.2.1 VCCRTC External Circuit

On XBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCPSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

SSID = Thermal Sensor

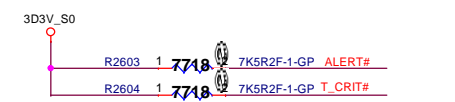


2016/12/21 change PN

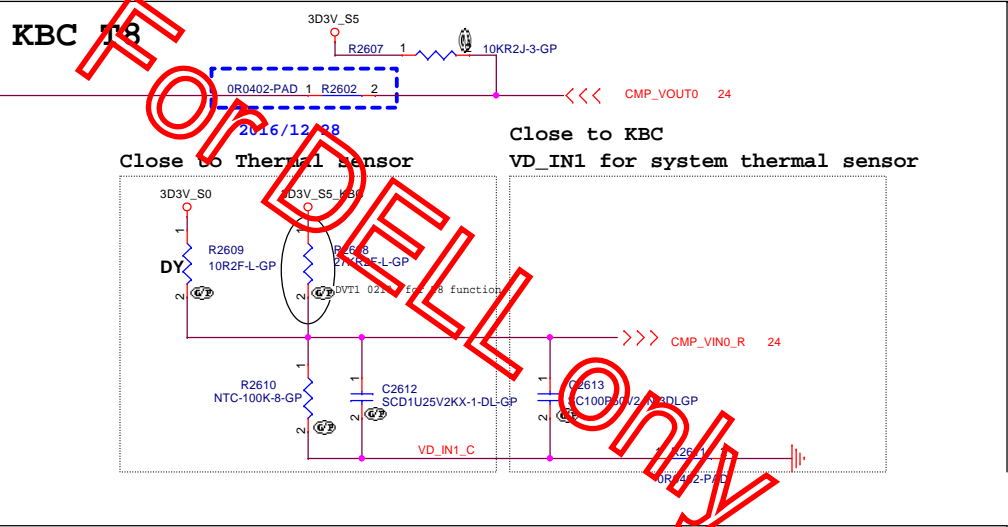


Layout Note:
C2607 close THM2601

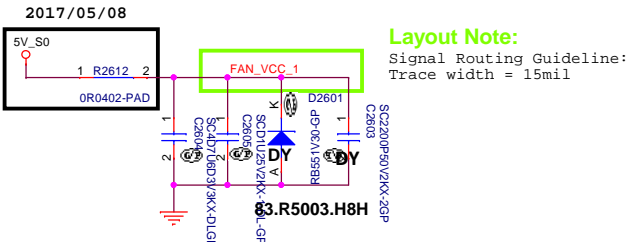
Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



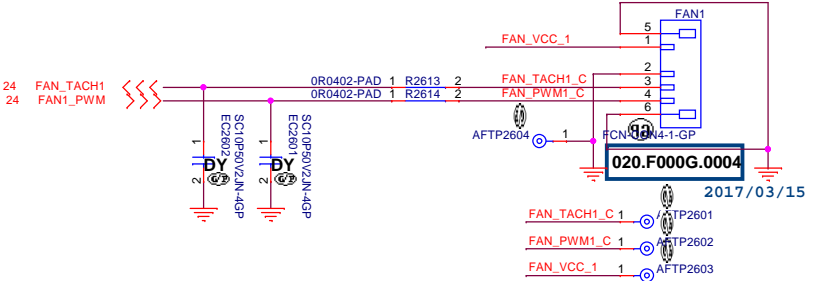
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

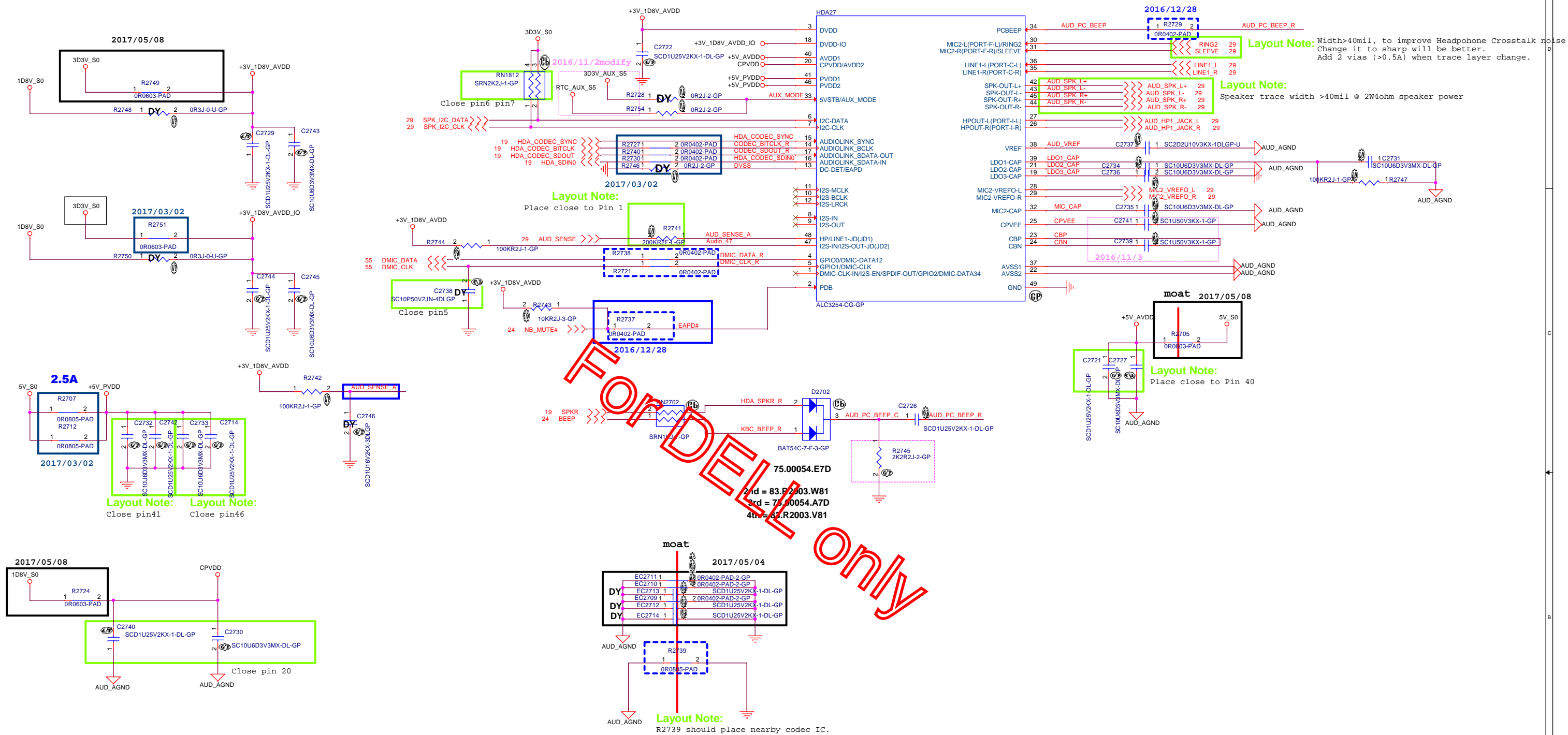


PWM FAN1



Layout Note:
Signal Routing Guideline:
Trace width = 15mil






5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

(Blanking)
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Title

(Reserved)


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5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)

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<Core Design>

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Title (Reserved)			
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5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)

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Title


LAN RTL8106

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5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)
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Title

XFOM&RJ45

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5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)
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<Core Design>



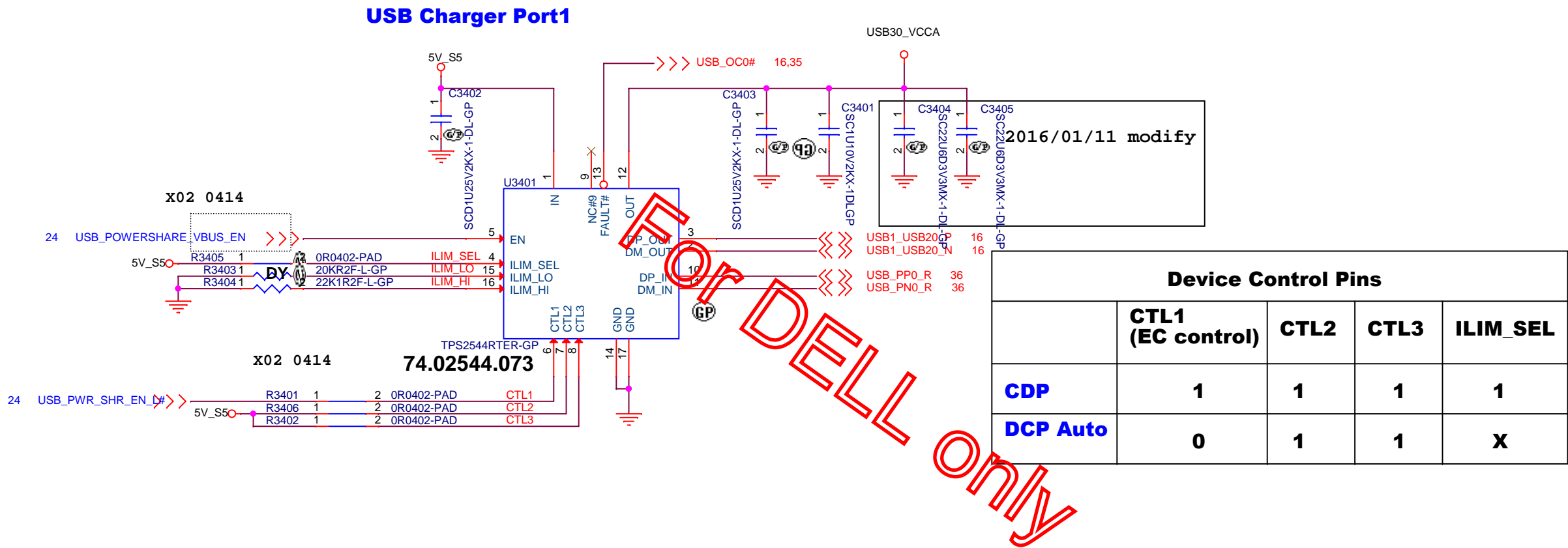
Wistron Corporation

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Title

Card Reader-RTS5170

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Title

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Size
A3

Document Number

KyloRen 13"

Rev

A00

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Sheet

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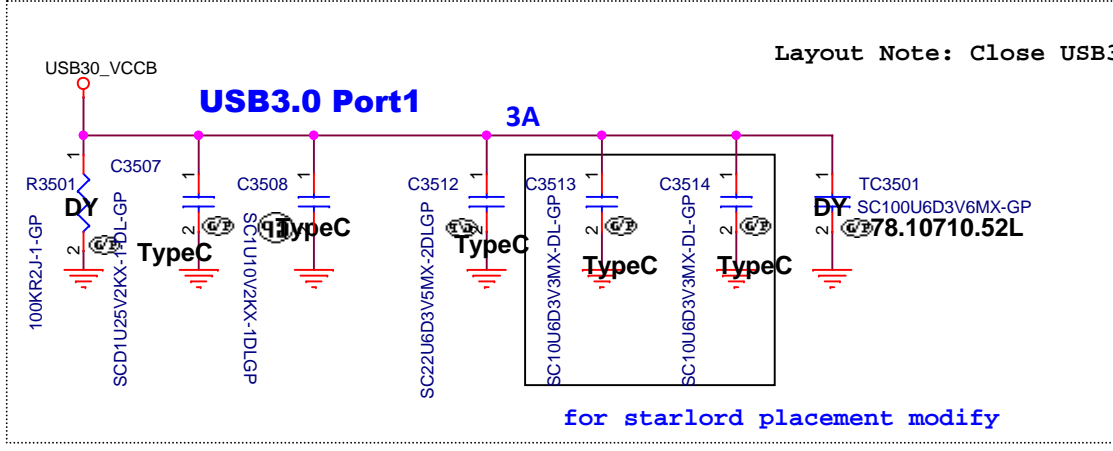
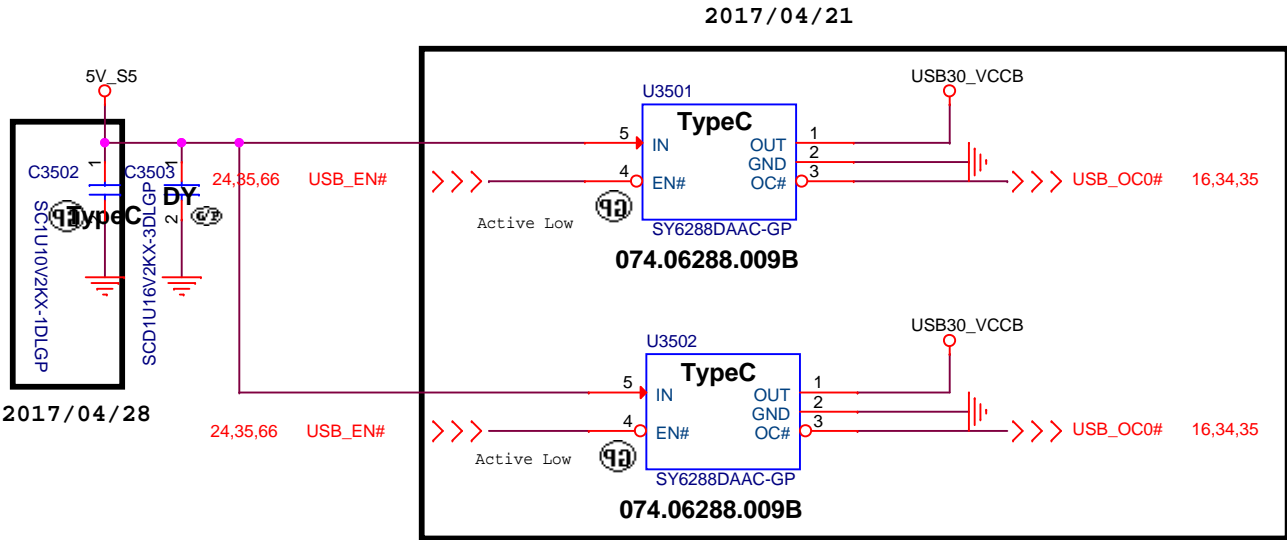
of

106

SSID = USB3.0 Port1

USB Port1 Type-C

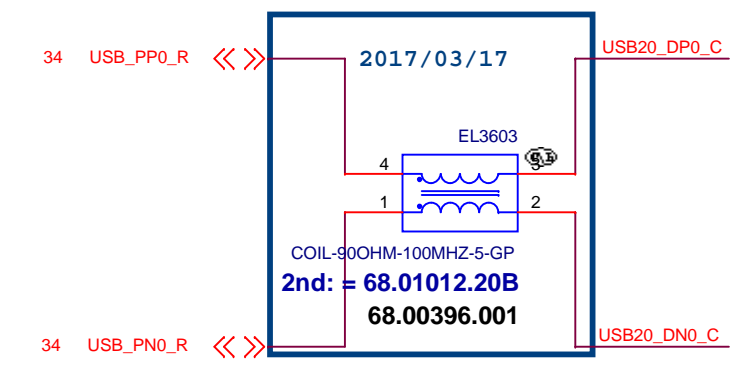
USB 3.0 Port3



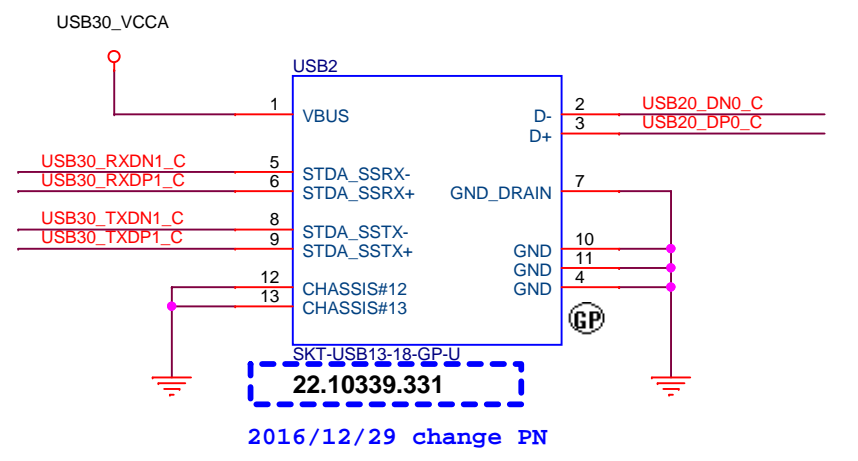
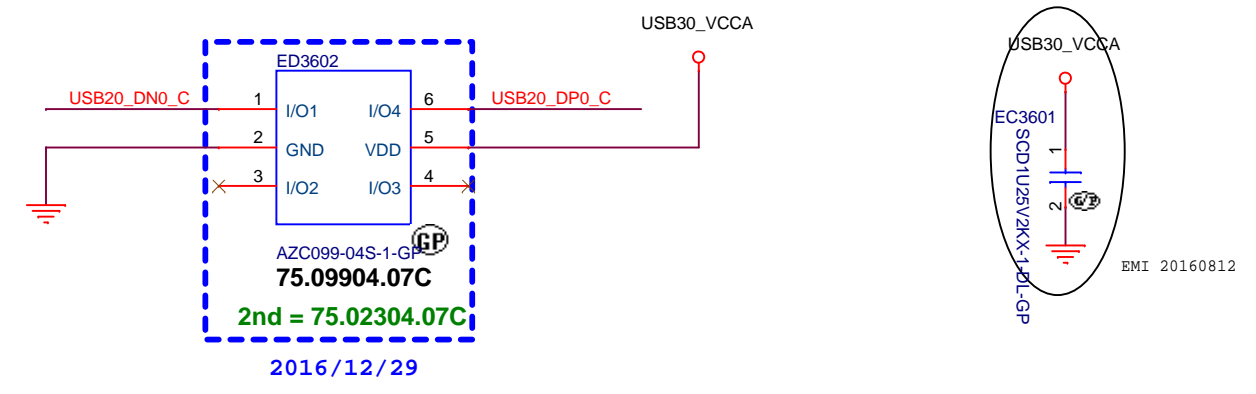
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SSID = USB3.0 Port1

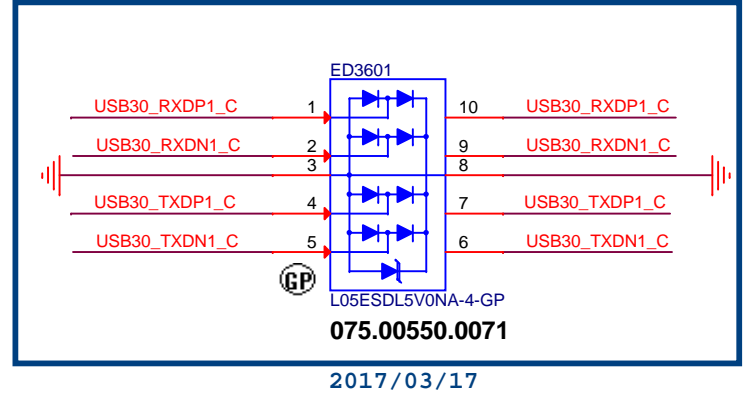
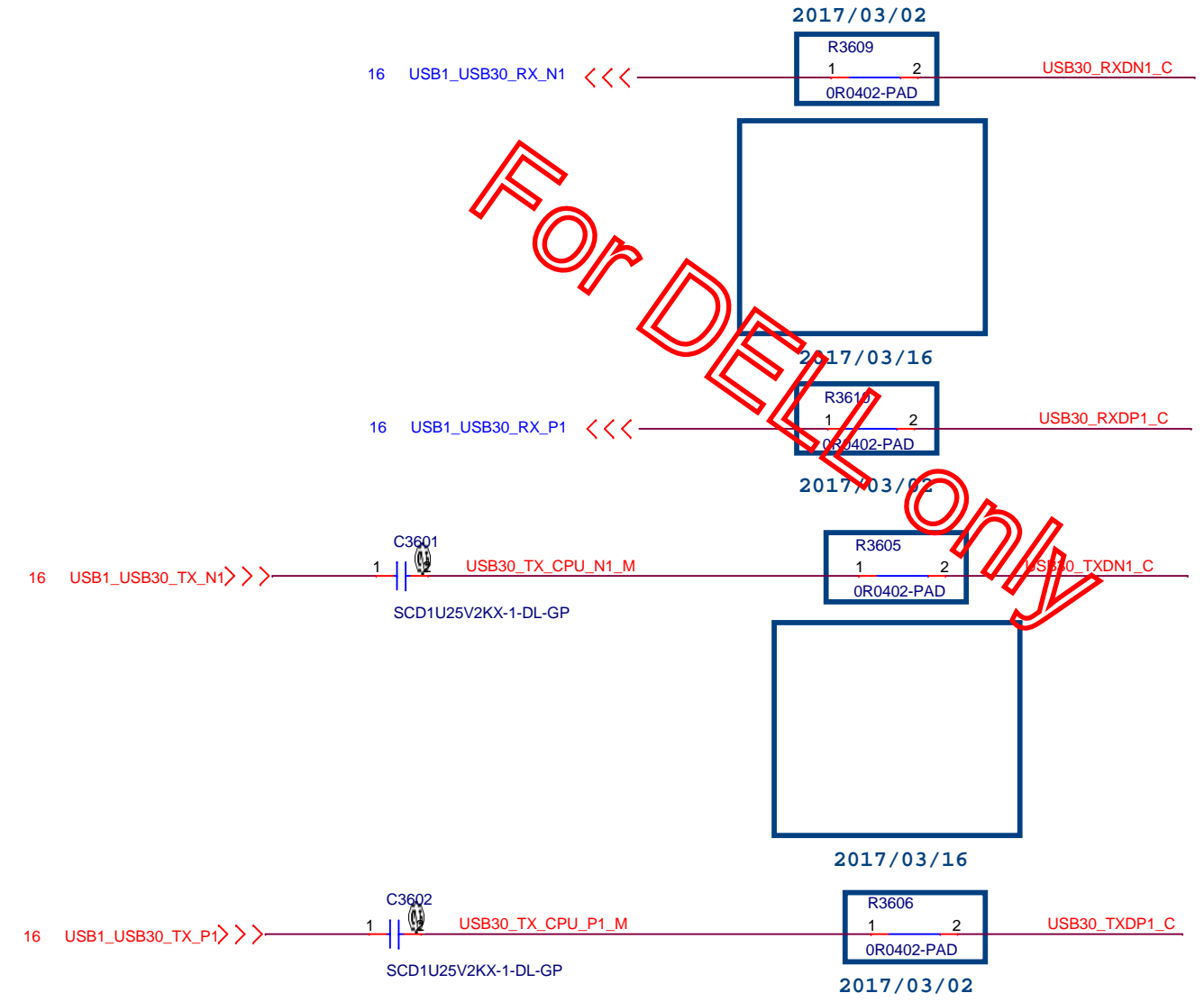
USB3.0 Port1



USB2.0 Port2 and USB2.0 Port3 are on IOBD



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



SSID = TYPEC MUX



FLP	CRS	CRS	CRS	Mux Operation
ANSEL	ANSEL	ANSEL	AN	
X	LOW	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23	CTLI/HPFDIN HPD in 12C mode	HPD Enable in GPIO mode, Unused in 12C mode
29	CAD_SNK/DCI_DAT AUX Snoop EN in GPIO mode DCI DAT in 12C mode	AUX Snoop EN in GPIO mode EN in 12C mode
32	DCI_CLK HPD in GPIO mode DCI_CLK in 12C mode	HPD

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

(Blanking)

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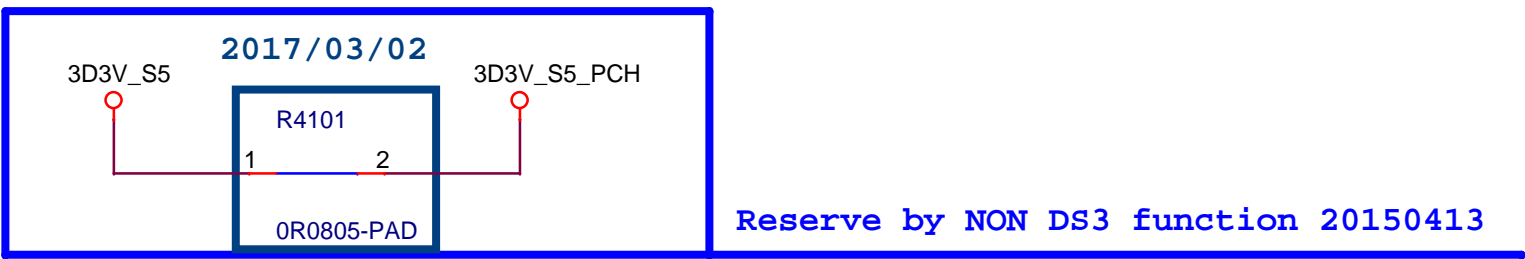
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Title

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SSID = Power Plane & Sequence



DS3

<Core Design>


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Title Connected_Standby(1/2)+DS3			
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5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)

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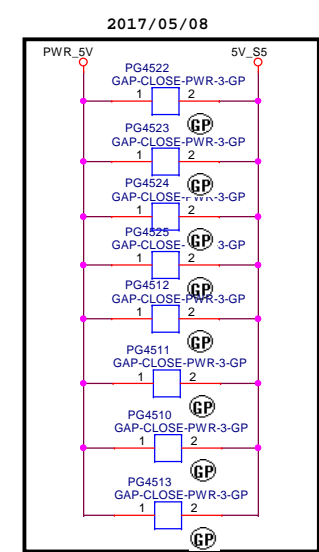
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Connected_Standby(2/2)			
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Pin Definition: TBD

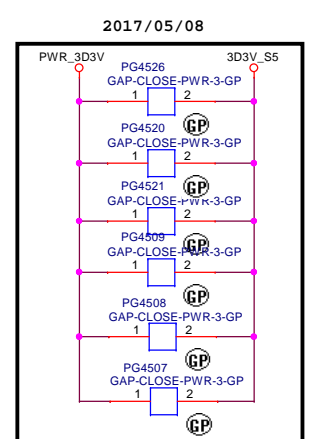



```
SSID = PWR.Plane.Regulator_3D3V
```



EN rating 25V
EN Rising Threshold : 0.8V
I_{limt} : 8A

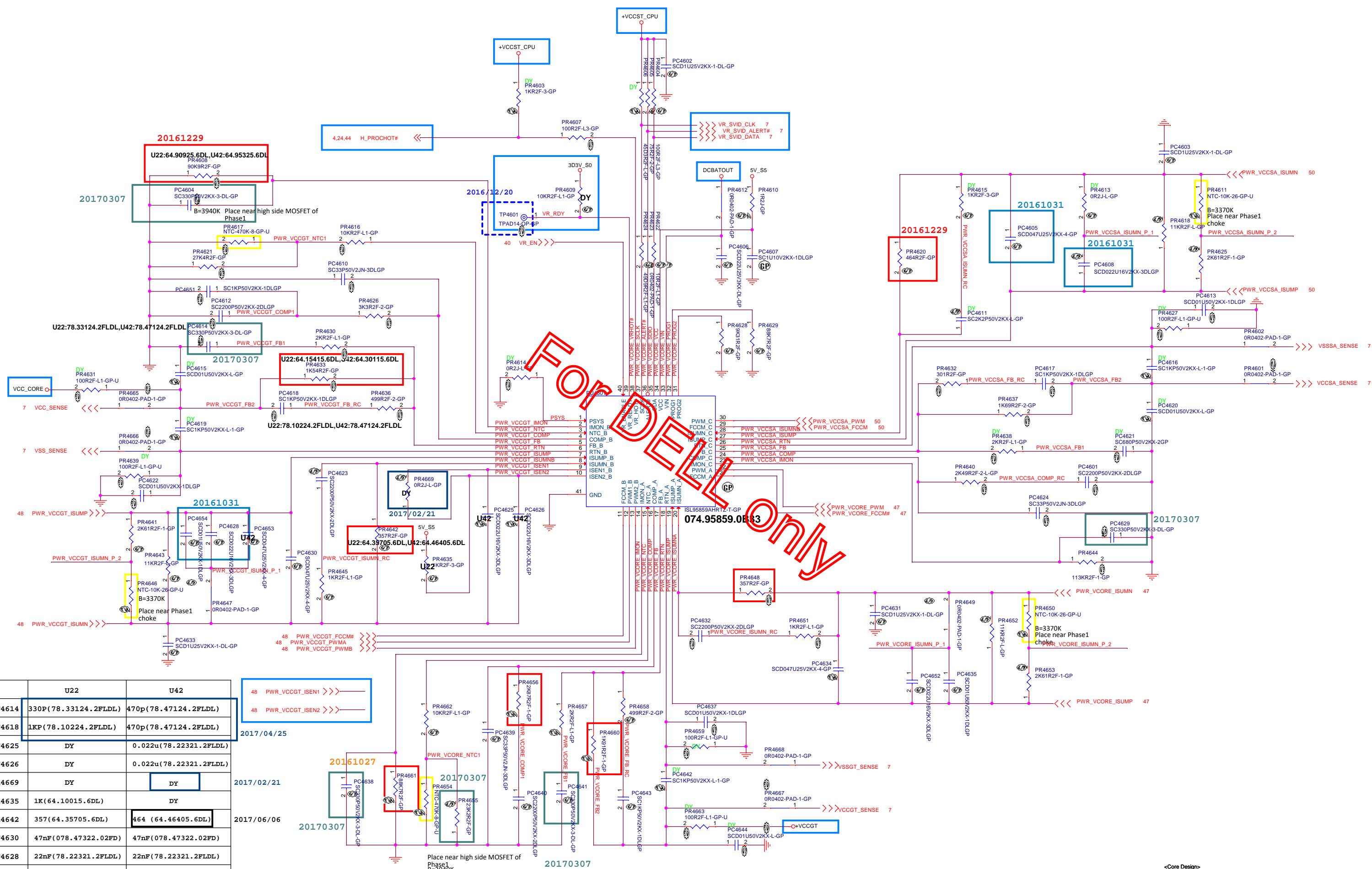
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EN rating 25V
EN Rising Threshold : 0.8V
I_{limt} : 8A

RF request 2016/01/12 modify

Main Func = CPU_CORE



	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	464 (64.46405.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	10nF(78.10324.2FLDL)	10nF(78.10324.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	3.01K(64.30115.6DL)
PR4608	90.9K(64.90925.6DL)	95.3K (64.95325.6DL)

<Core Design>

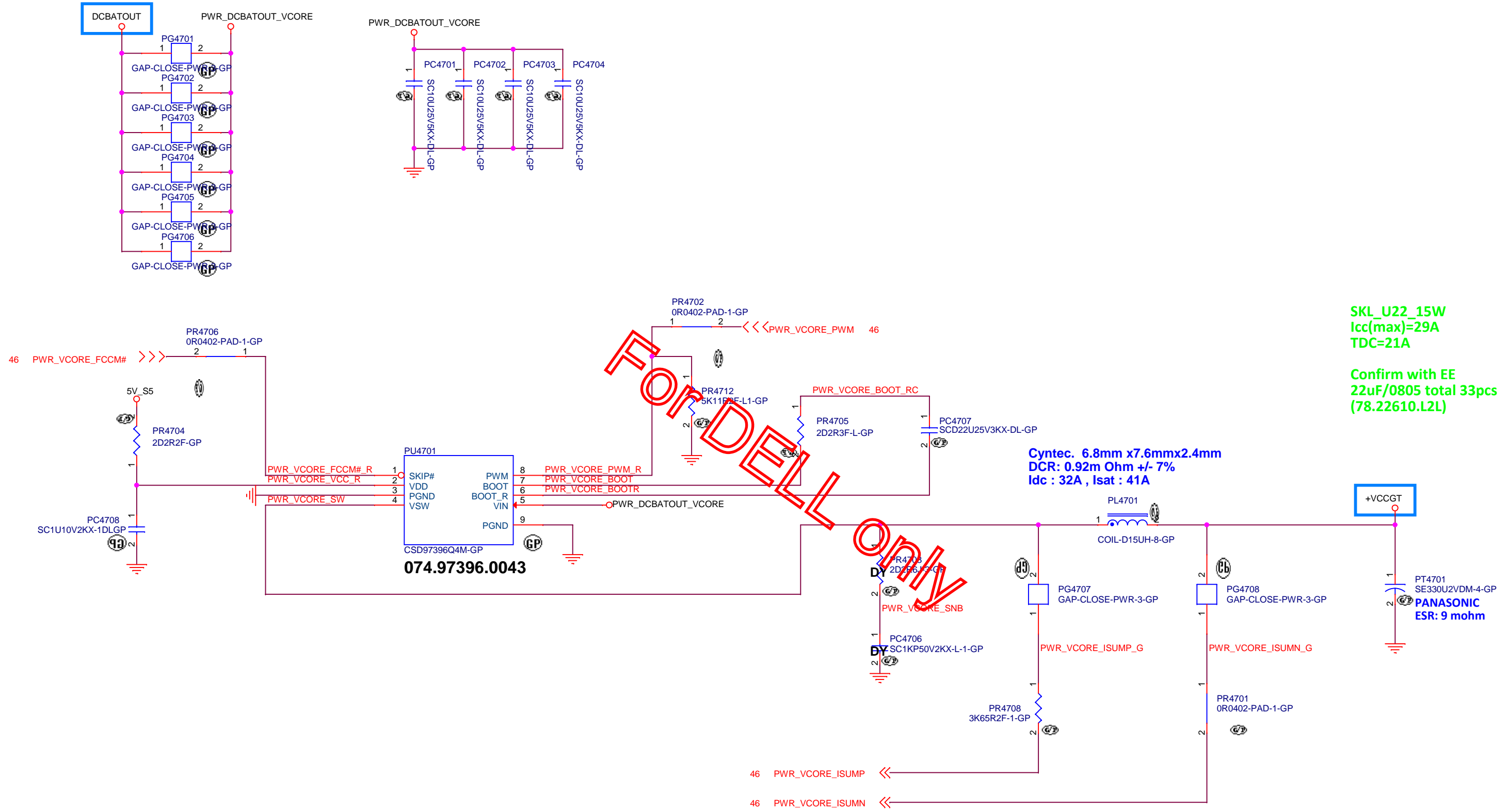


Title **NCP81208MN CPU VCORE(1/3)**

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SSID = CPU_CORE



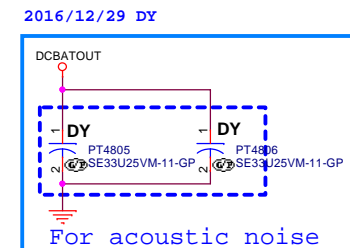
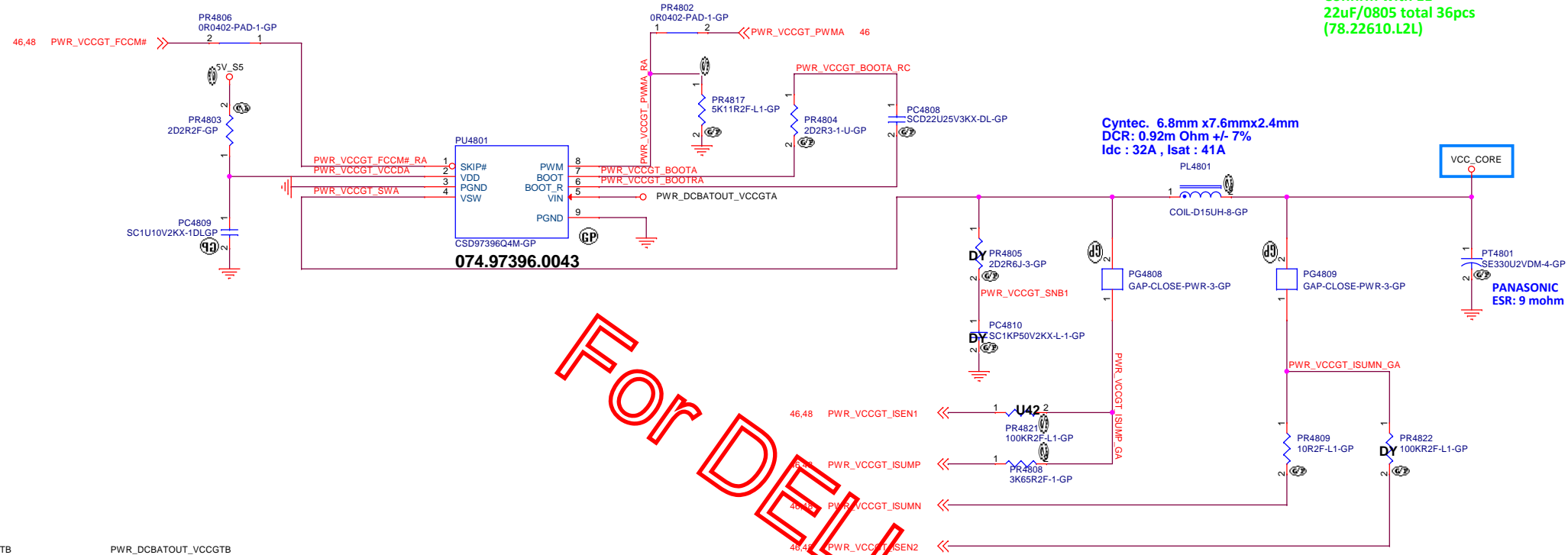
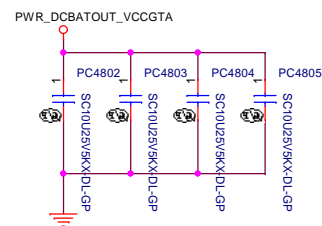
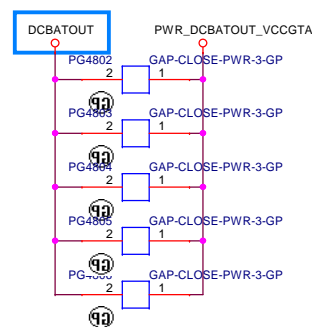
SKL_U22_15W
Icc(max)=29A
TDC=21A

Confirm with EE
22uF/0805 total 33pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.92m Ohm +/- 7%
Idc : 32A , Isat : 41A

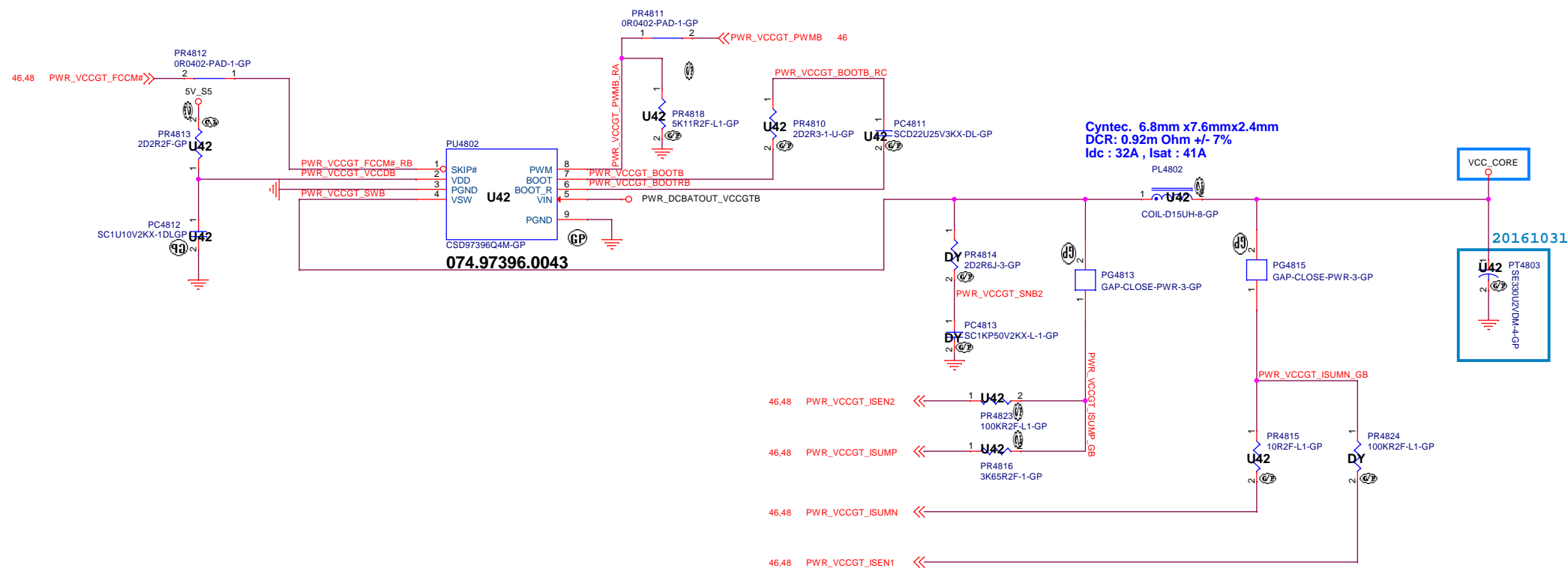
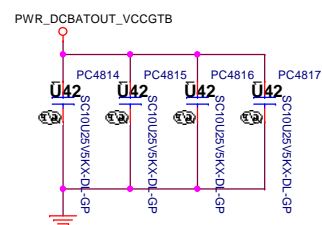
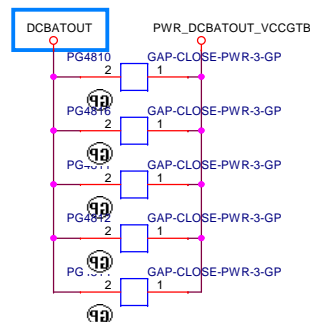
PANASONIC
ESR: 9 mohm

Main Func = CPU_CORE



KBL_U42_15W
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



<Core Design>



Title **NCP81382MN CPU VCCGT(3/3)**


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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		NCP81210MN_CPU_VCCGTUS	
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SSID = CPU_CORE

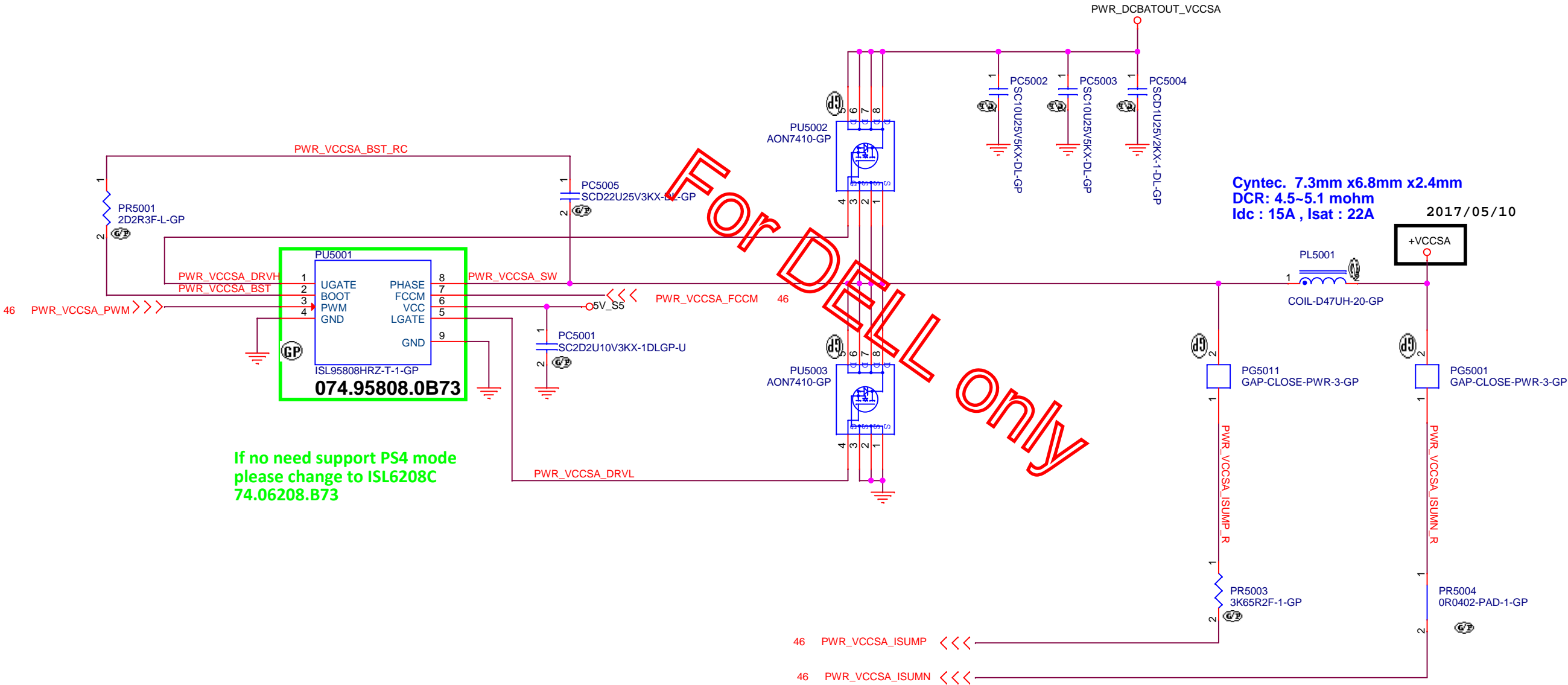
PWR_DCBATOUT_VCCSA 1

2017/03/16

2016/12/14 remove PT5001

SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)



If no need support PS4 mode
please change to ISL6208C
74.06208.B73

Cyntec. 7.3mm x6.8mm x2.4mm
DCR: 4.5~5.1 mohm
Idc : 15A , Isat : 22A

2017/05/10

<Core Design>

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Title VCCSA					
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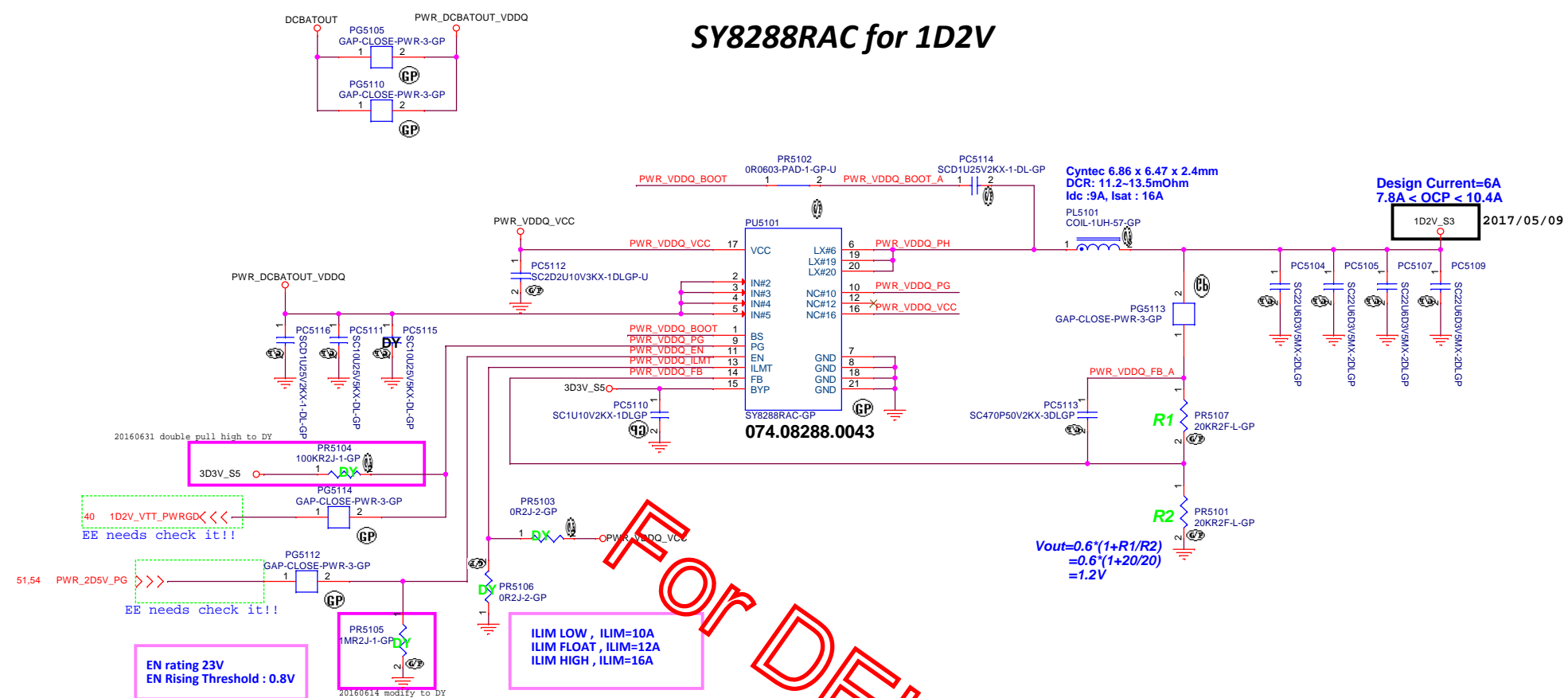
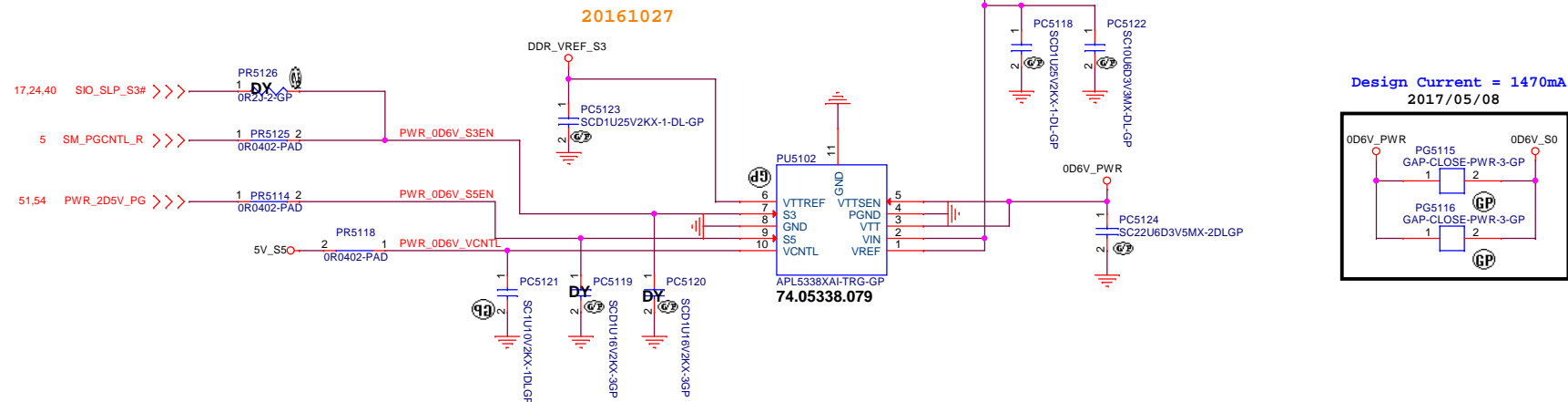


Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

APL5338 for 0D6V

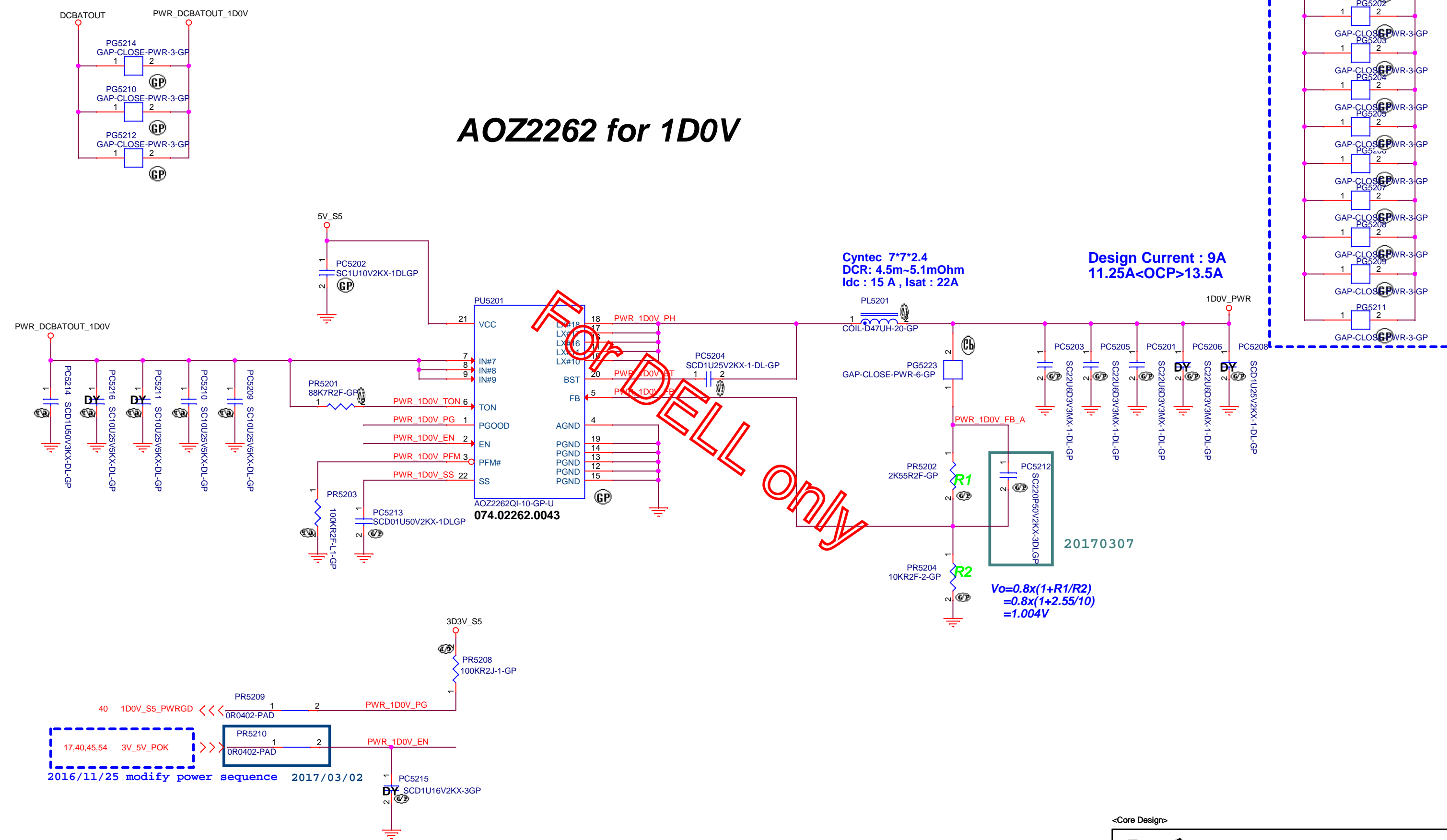


EE needs check it!!

<Core Design>

SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V



A	B	C	D	E
4				4
3				3
2				2
1				1
A	B	C	D	E

(Blanking)

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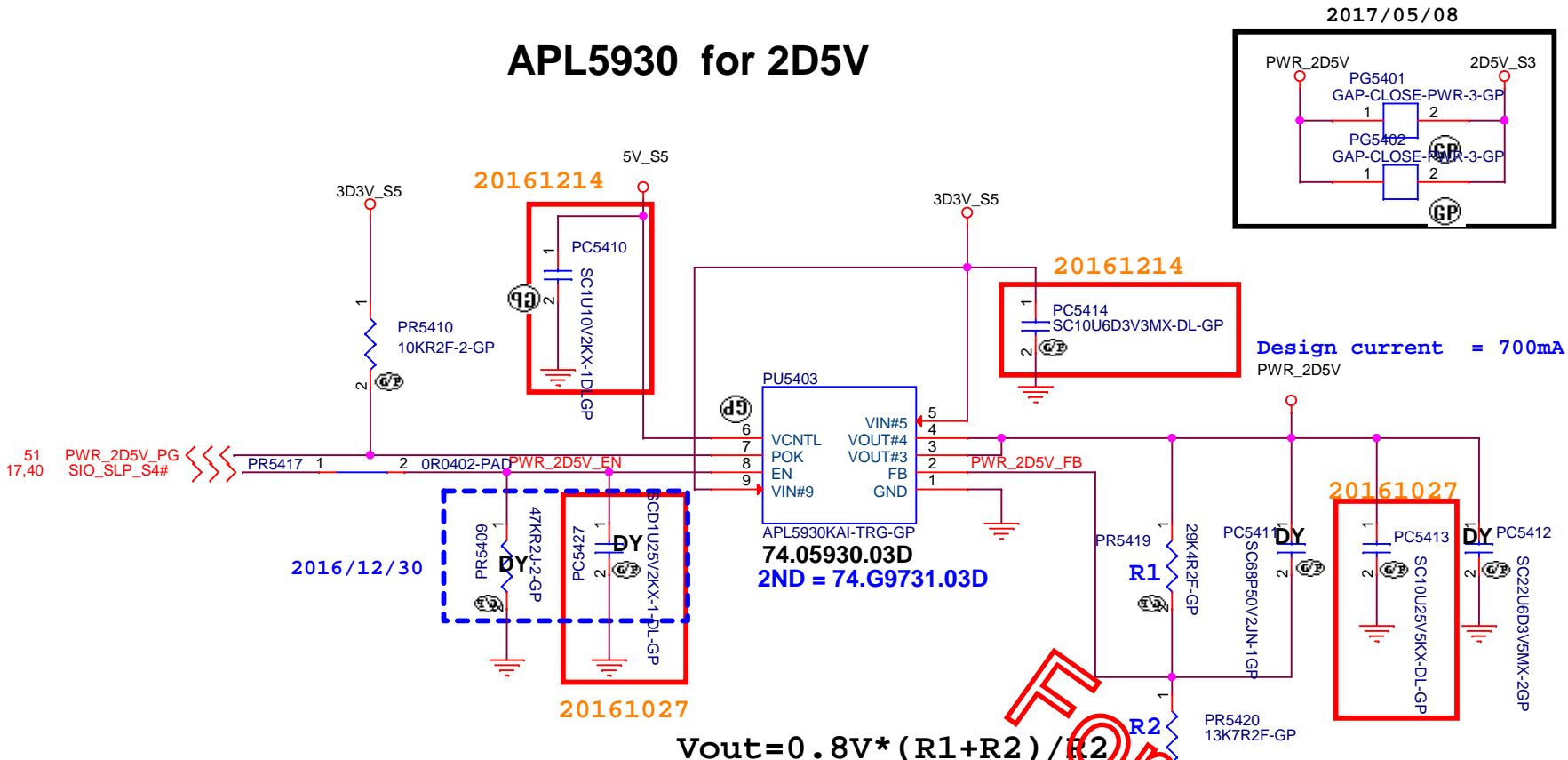
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Taipei Hsien 221, Taiwan, R.O.C.

Title

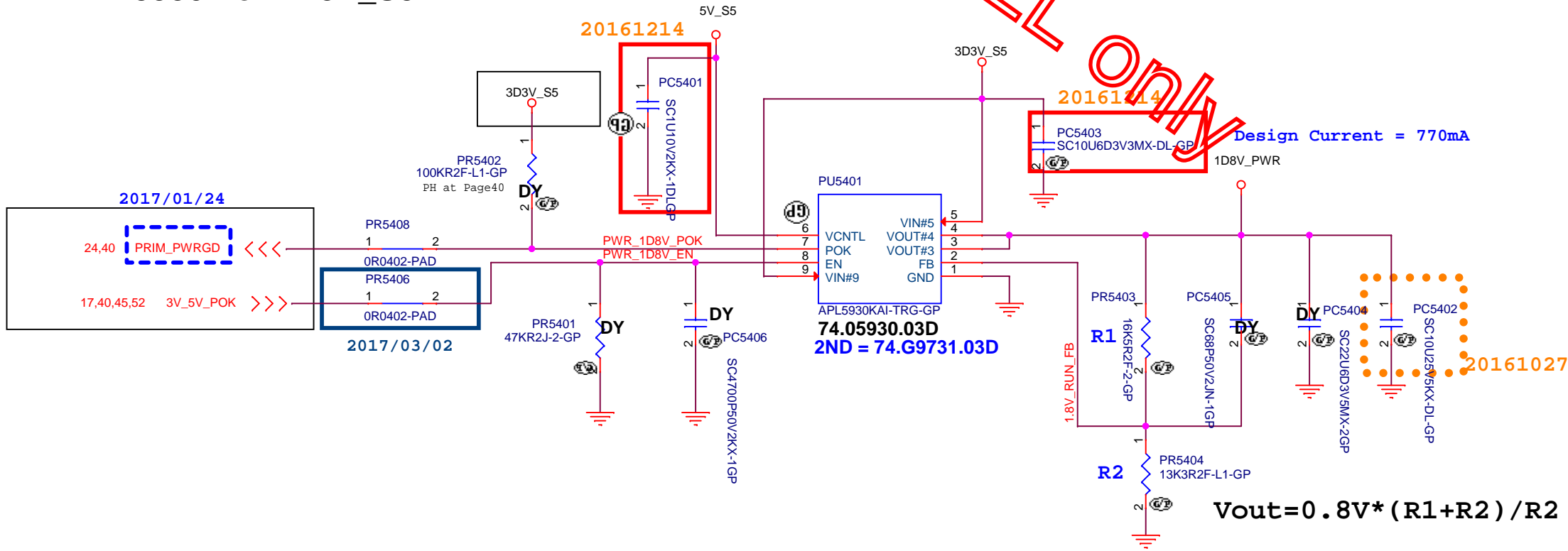
(Reserved)

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APL5930 for 2D5V



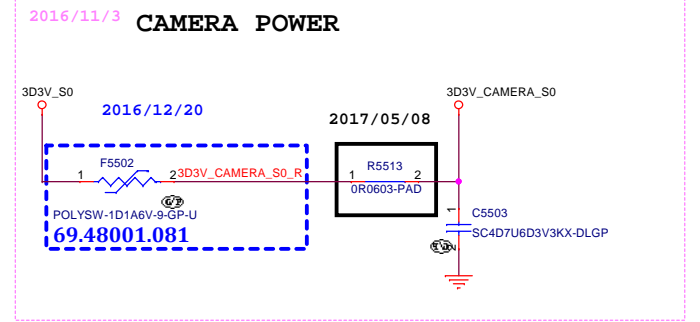
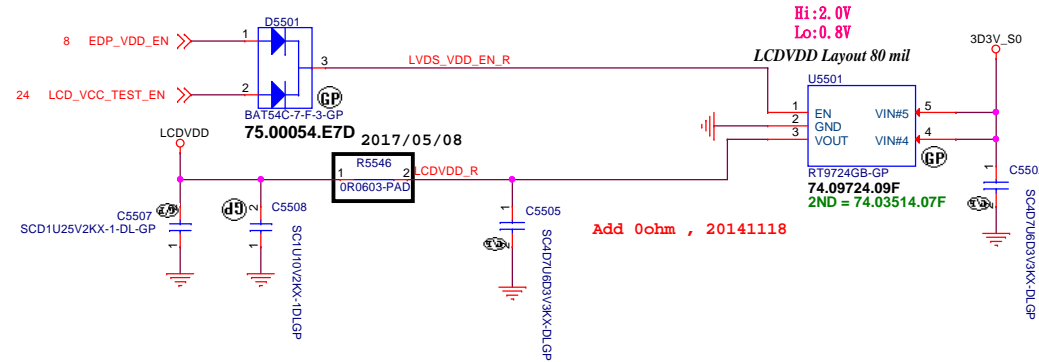
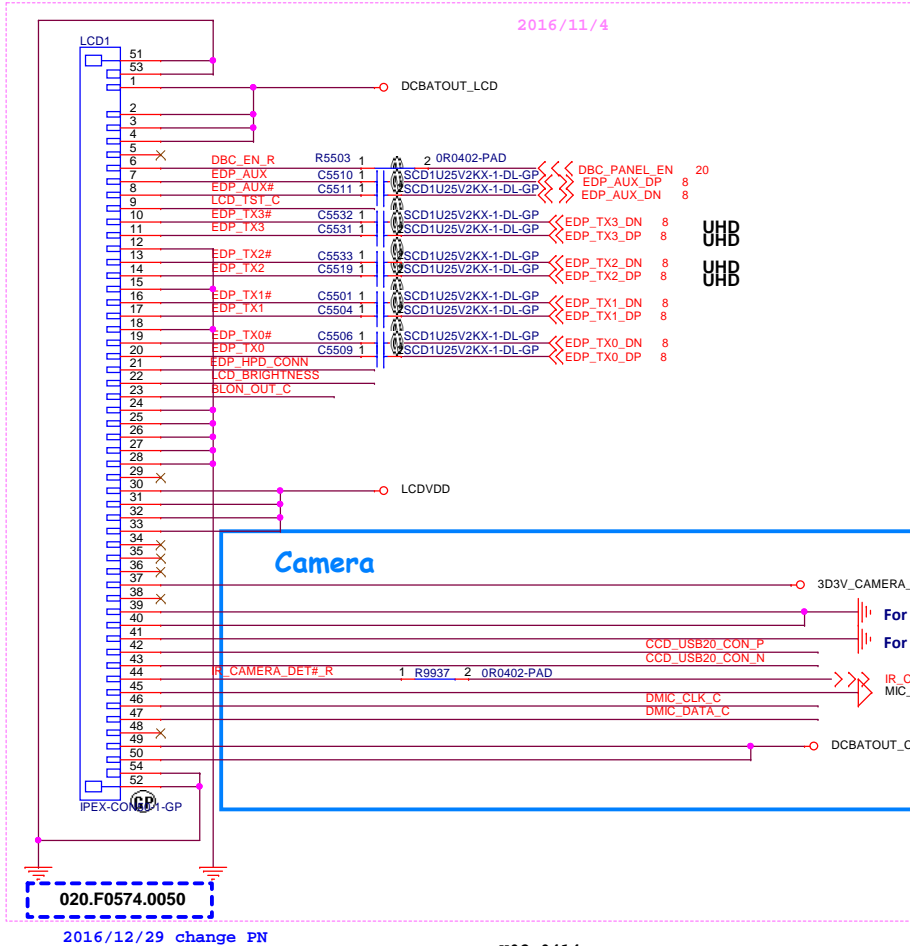
APL5930 for 1D8V_S5



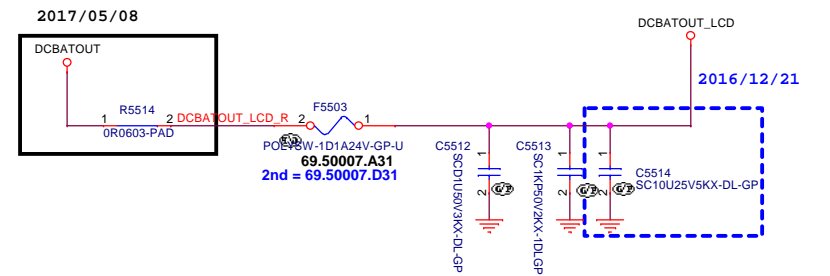
<Core Design>

SSID = LCD

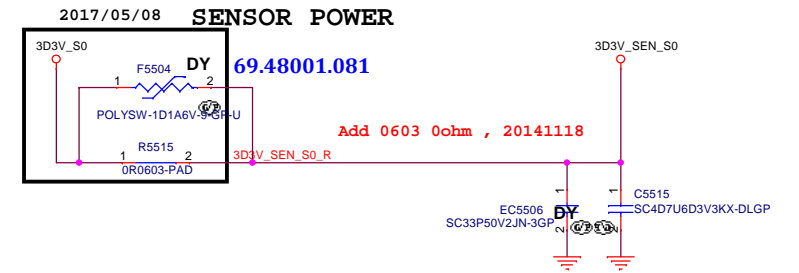
Panel / Camera/ DMIC



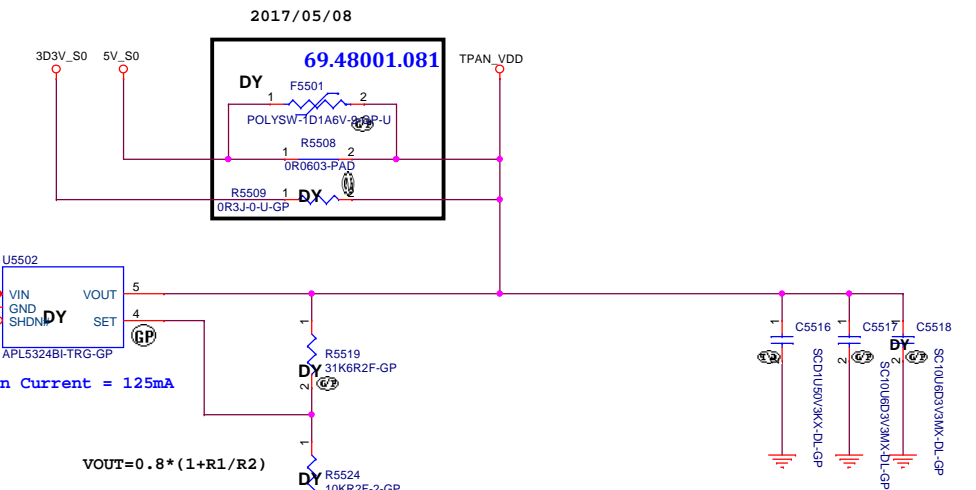
INVERTER POWER



Starload height limite change to 0603 package
2015/09/24 modify

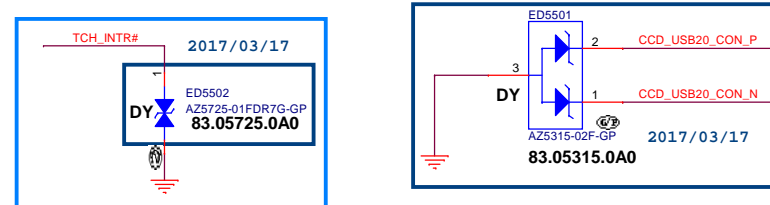
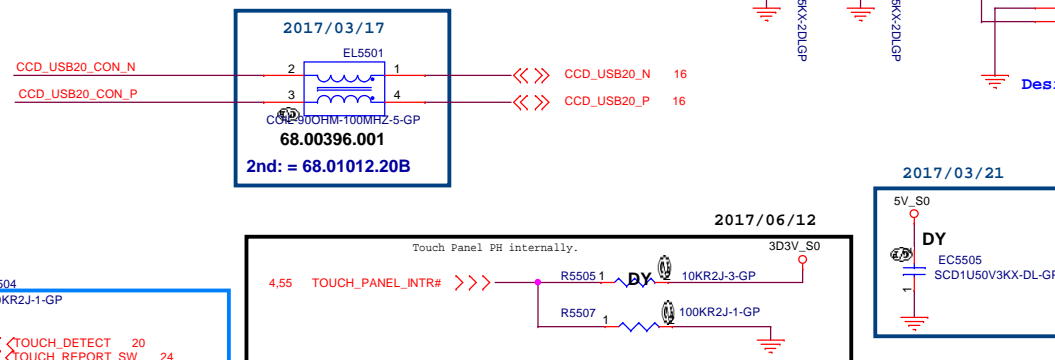
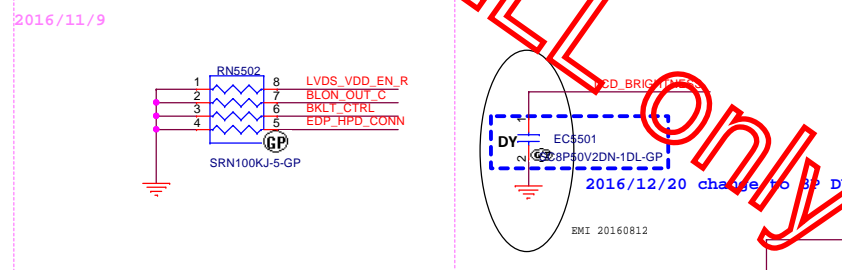
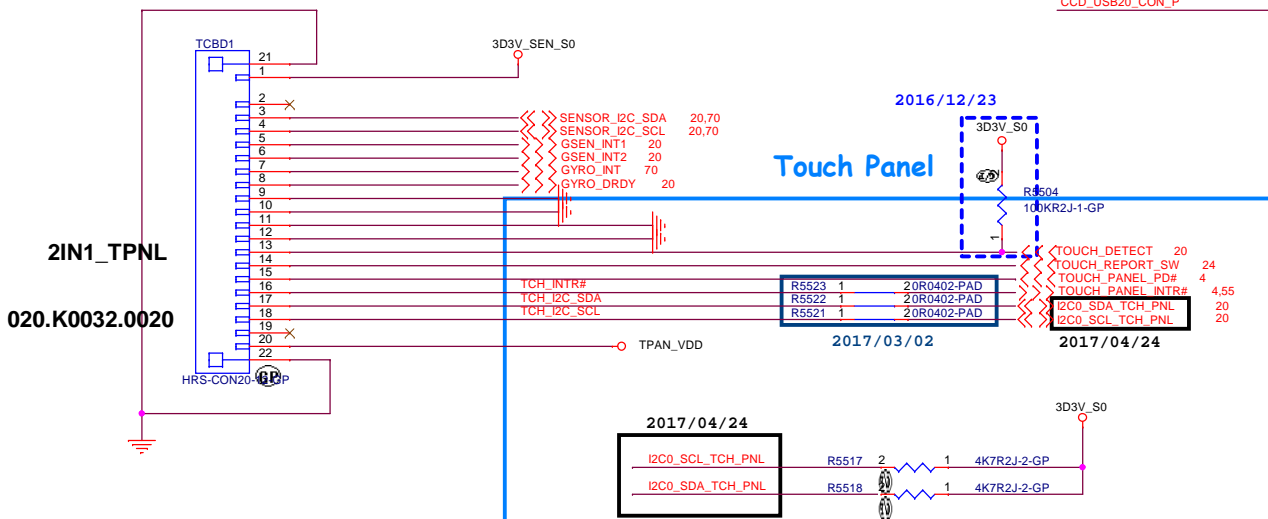


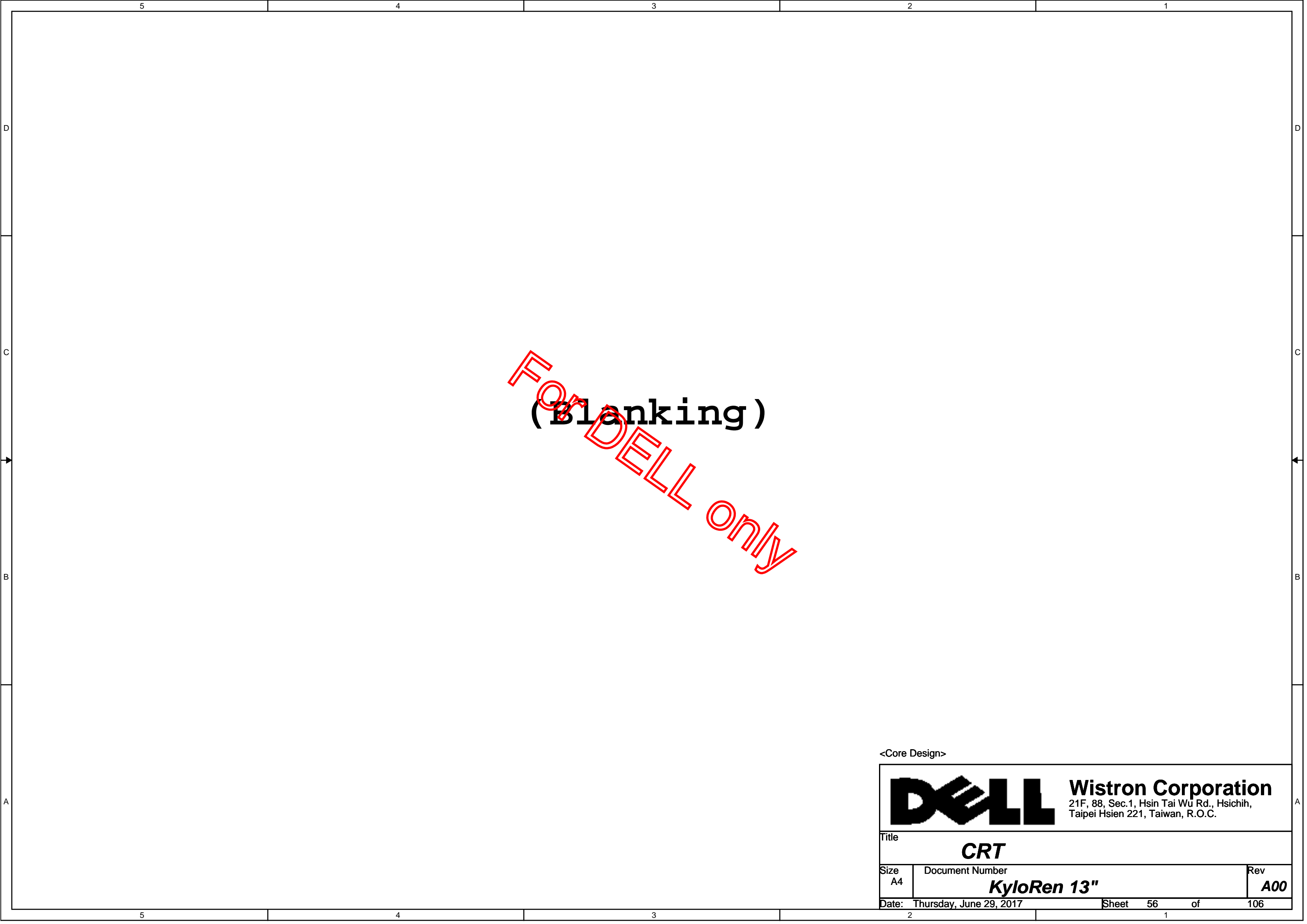
TOUCH PANEL POWER



Starload height limite change to 0603 package
2015/09/30 modify

Sensor/ Touch Panel






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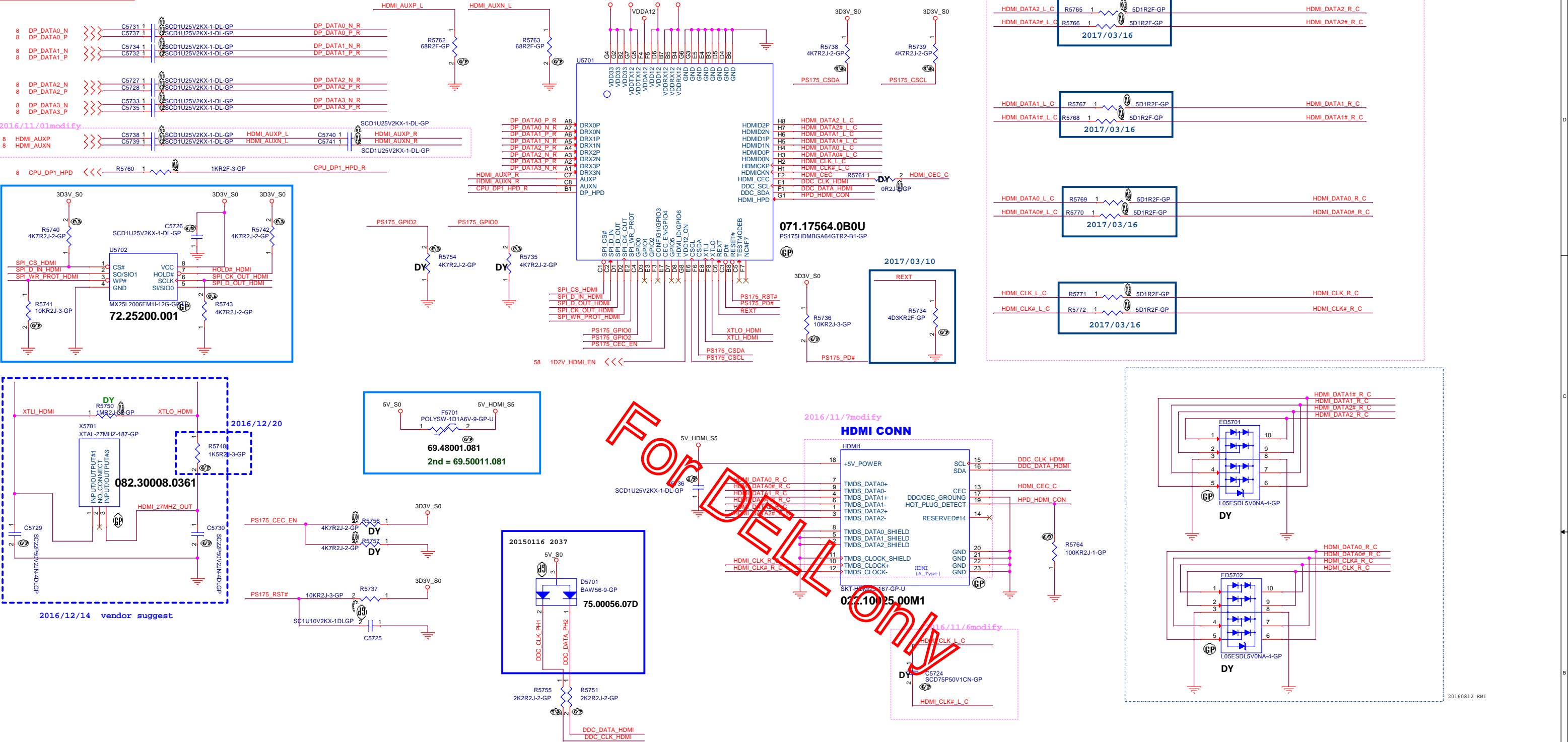
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Title

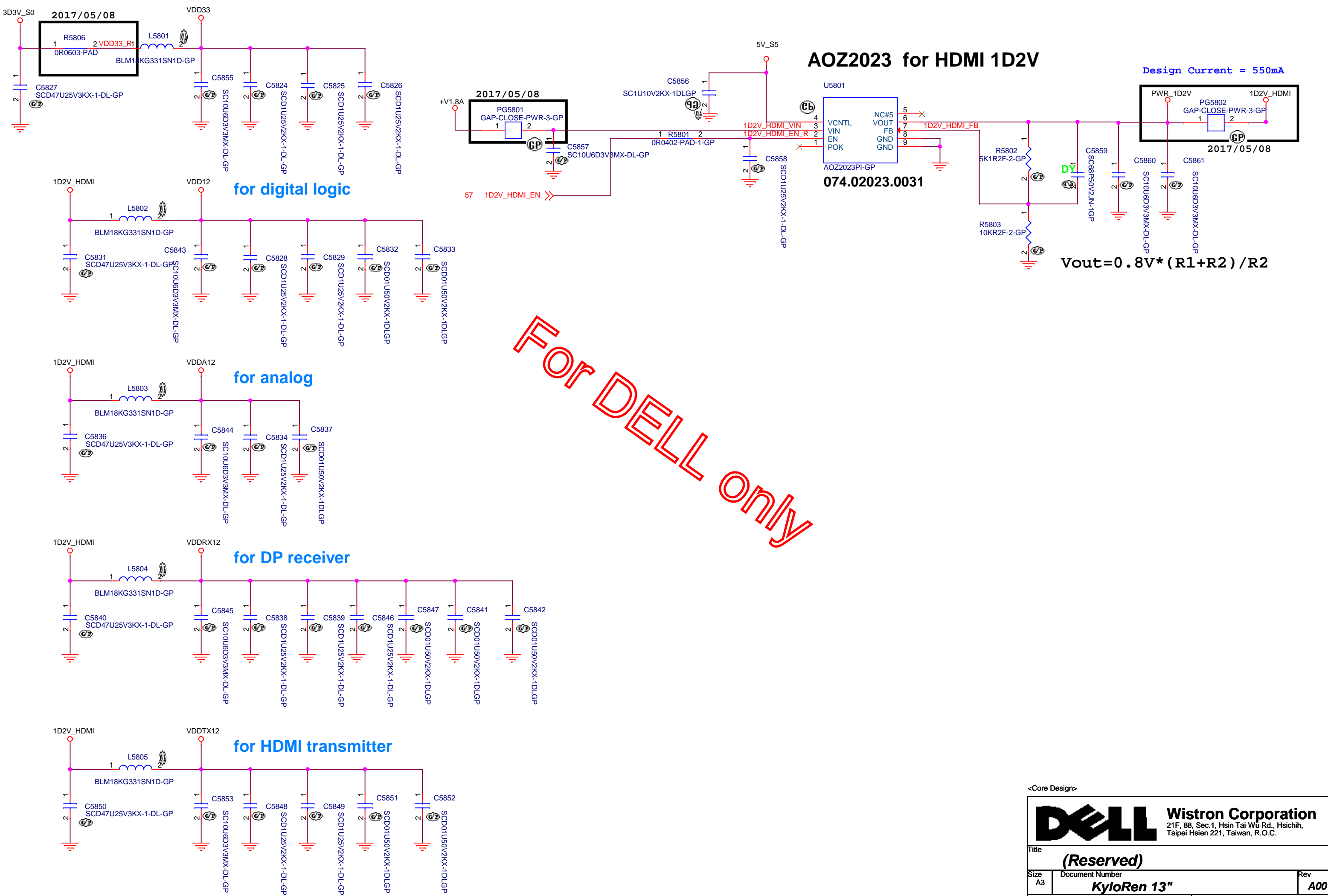
CRT

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SSID = HDMI




SSID = HDMI



5	4	3	2	1
D				D
C				C
B				B
A				A

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Title (Reserved)			
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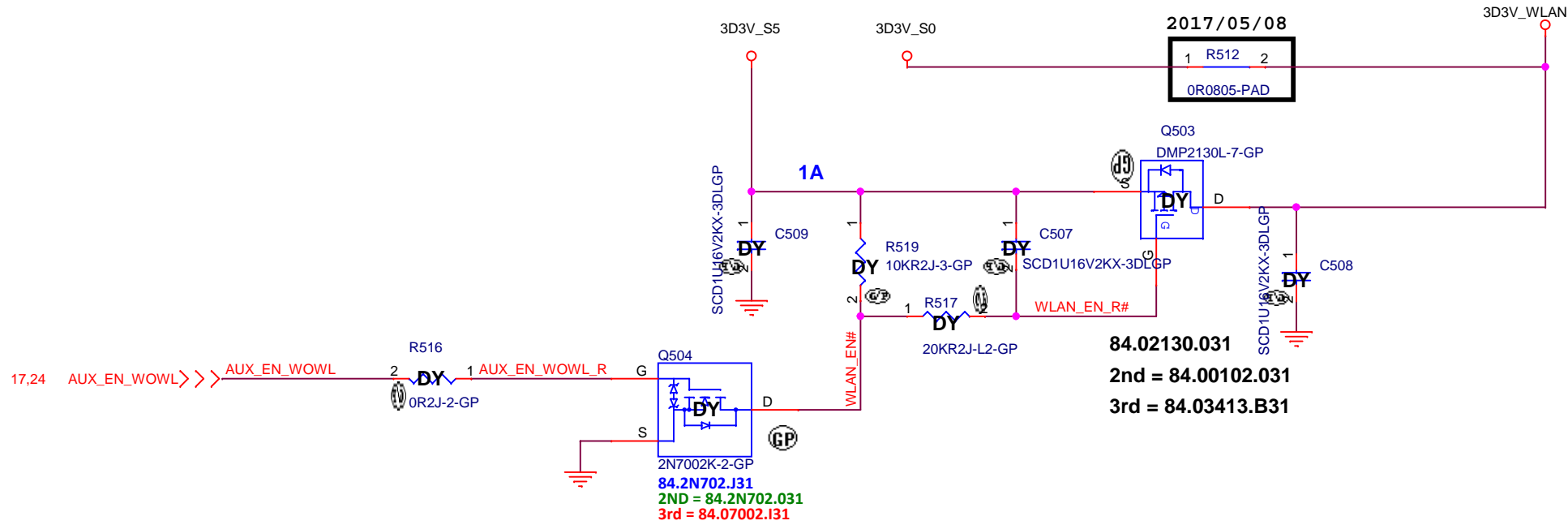
	5	4	3	2	1
E					
D					
C					
B					
A					

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Title			
<i>SATA IF HDD/ODD</i>			
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SSID = WLAN



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A	B	C	D	E
4				4
3				3
2				2
1				1
A	B	C	D	E

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Title

Reserved

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SSID = M.2

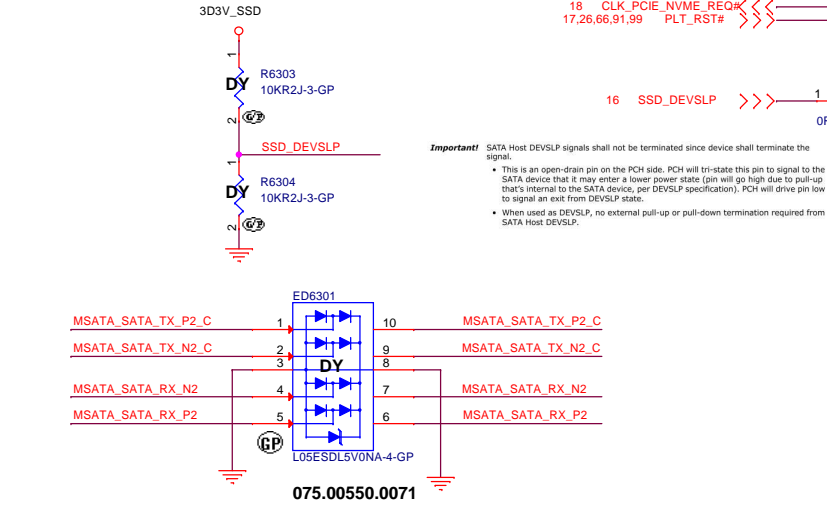
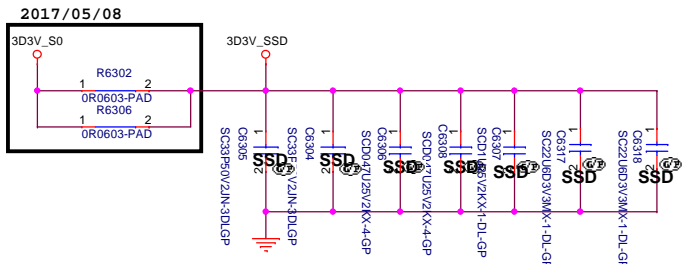
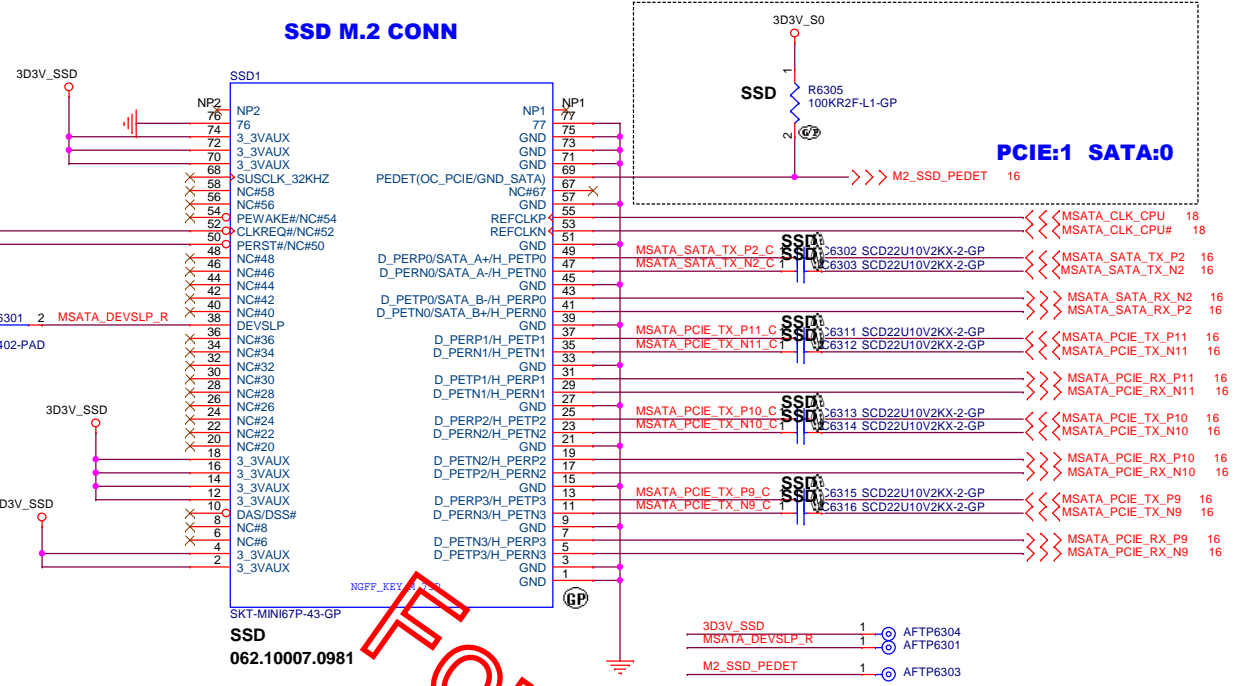


Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

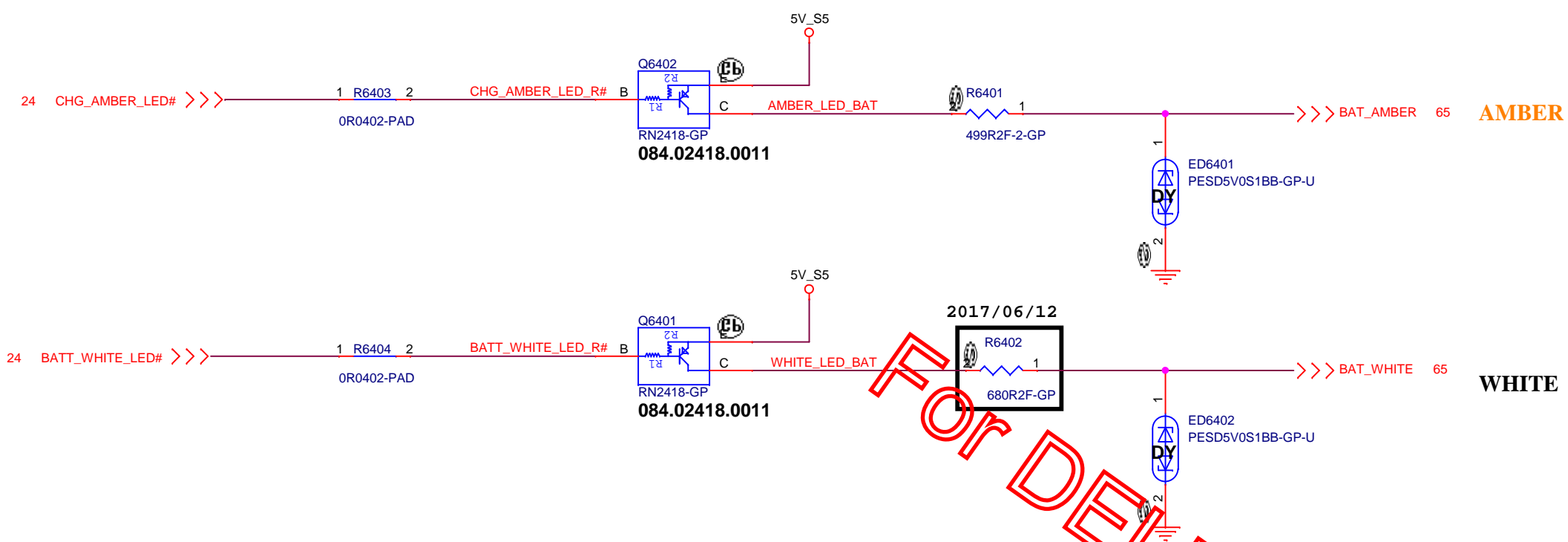


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Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

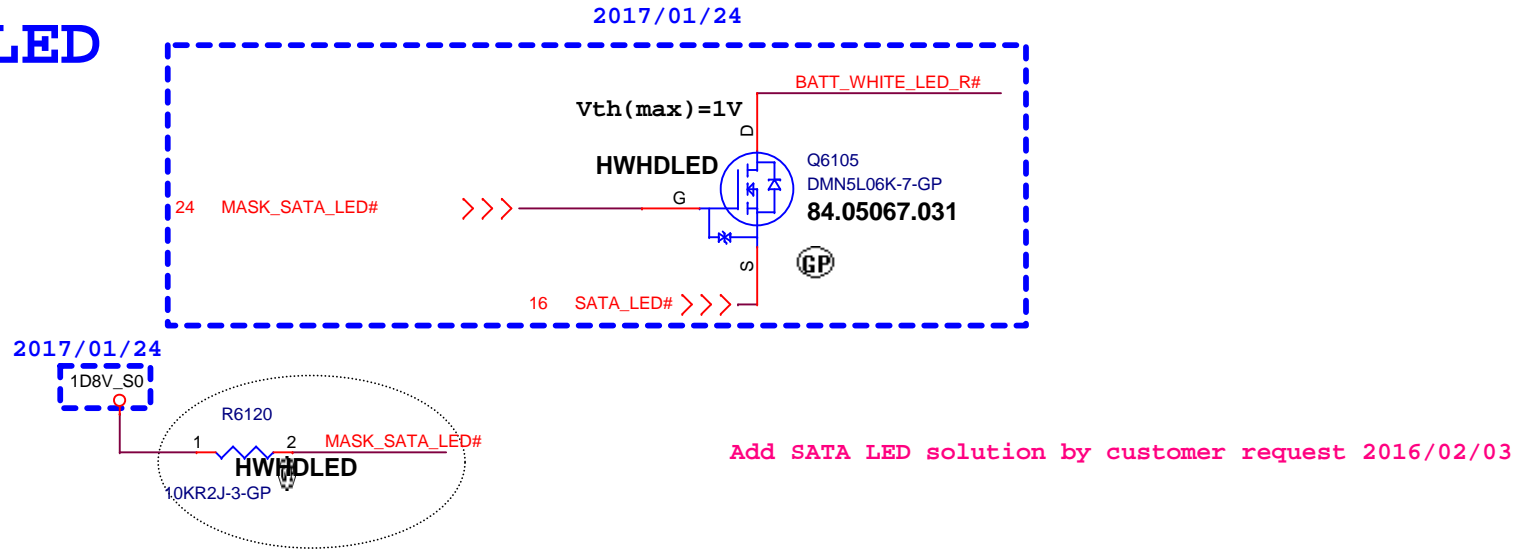
Pin	Signal	Pin	Signal
76	3.3V_AUX	77	3.3V_AUX
78	3.3V_AUX	79	3.3V_AUX
80	3.3V_AUX	81	3.3V_AUX
82	3.3V_AUX	83	3.3V_AUX
84	3.3V_AUX	85	3.3V_AUX
86	3.3V_AUX	87	3.3V_AUX
88	3.3V_AUX	89	3.3V_AUX
90	3.3V_AUX	91	3.3V_AUX
92	3.3V_AUX	93	3.3V_AUX
94	3.3V_AUX	95	3.3V_AUX
96	3.3V_AUX	97	3.3V_AUX
98	3.3V_AUX	99	3.3V_AUX
100	3.3V_AUX	101	3.3V_AUX
102	3.3V_AUX	103	3.3V_AUX
104	3.3V_AUX	105	3.3V_AUX
106	3.3V_AUX	107	3.3V_AUX
108	3.3V_AUX	109	3.3V_AUX
110	3.3V_AUX	111	3.3V_AUX
112	3.3V_AUX	113	3.3V_AUX
114	3.3V_AUX	115	3.3V_AUX
116	3.3V_AUX	117	3.3V_AUX
118	3.3V_AUX	119	3.3V_AUX
120	3.3V_AUX	121	3.3V_AUX
122	3.3V_AUX	123	3.3V_AUX
124	3.3V_AUX	125	3.3V_AUX
126	3.3V_AUX	127	3.3V_AUX
128	3.3V_AUX	129	3.3V_AUX
130	3.3V_AUX	131	3.3V_AUX
132	3.3V_AUX	133	3.3V_AUX
134	3.3V_AUX	135	3.3V_AUX
136	3.3V_AUX	137	3.3V_AUX
138	3.3V_AUX	139	3.3V_AUX
140	3.3V_AUX	141	3.3V_AUX
142	3.3V_AUX	143	3.3V_AUX
144	3.3V_AUX	145	3.3V_AUX
146	3.3V_AUX	147	3.3V_AUX
148	3.3V_AUX	149	3.3V_AUX
150	3.3V_AUX	151	3.3V_AUX
152	3.3V_AUX	153	3.3V_AUX
154	3.3V_AUX	155	3.3V_AUX
156	3.3V_AUX	157	3.3V_AUX
158	3.3V_AUX	159	3.3V_AUX
160	3.3V_AUX	161	3.3V_AUX
162	3.3V_AUX	163	3.3V_AUX
164	3.3V_AUX	165	3.3V_AUX
166	3.3V_AUX	167	3.3V_AUX
168	3.3V_AUX	169	3.3V_AUX
170	3.3V_AUX	171	3.3V_AUX
172	3.3V_AUX	173	3.3V_AUX
174	3.3V_AUX	175	3.3V_AUX
176	3.3V_AUX	177	3.3V_AUX
178	3.3V_AUX	179	3.3V_AUX
180	3.3V_AUX	181	3.3V_AUX
182	3.3V_AUX	183	3.3V_AUX
184	3.3V_AUX	185	3.3V_AUX
186	3.3V_AUX	187	3.3V_AUX
188	3.3V_AUX	189	3.3V_AUX
190	3.3V_AUX	191	3.3V_AUX
192	3.3V_AUX	193	3.3V_AUX
194	3.3V_AUX	195	3.3V_AUX
196	3.3V_AUX	197	3.3V_AUX
198	3.3V_AUX	199	3.3V_AUX
200	3.3V_AUX	201	3.3V_AUX
202	3.3V_AUX	203	3.3V_AUX
204	3.3V_AUX	205	3.3V_AUX
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208	3.3V_AUX	209	3.3V_AUX
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212	3.3V_AUX	213	3.3V_AUX
214	3.3V_AUX	215	3.3V_AUX
216	3.3V_AUX	217	3.3V_AUX
218	3.3V_AUX	219	3.3V_AUX
220	3.3V_AUX	221	3.3V_AUX
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224	3.3V_AUX	225	3.3V_AUX
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254	3.3V_AUX	255	3.3V_AUX
256	3.3V_AUX	257	3.3V_AUX
258	3.3V_AUX	259	3.3V_AUX
260	3.3V_AUX	261	3.3V_AUX
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264	3.3V_AUX	265	3.3V_AUX
266	3.3V_AUX	267	3.3V_AUX
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270	3.3V_AUX	271	3.3V_AUX
272	3.3V_AUX	273	3.3V_AUX
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292	3.3V_AUX	293	3.3V_AUX
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334	3.3V_AUX	335	3.3V_AUX
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556	3.3V_AUX	557	3.3V_AUX
558	3.3V_AUX	559	3.3V_AUX
560	3.3V_AUX	561	3.3V_AUX
562	3.3V_AUX	563	3.3V_AUX
564	3.3V_AUX	565	3.3V_AUX
566	3.3V_AUX	567	3.3V_AUX
568	3.3V_AUX	569	3.3V_AUX
570	3.3V_AUX	571	3.3V_AUX
572	3.3V_AUX	573	3.3V_AUX
574	3.3V_AUX	575	3.3V_AUX
576	3.3V_AUX	577	3.3V_AUX
578	3.3V_AUX	579	3.3V_AUX
580	3.3V_AUX	581	3.3V_AUX
582	3.3V_AUX	583	3.3V_AUX
584	3.3V_AUX	585	3.3V_AUX
586	3.3V_AUX	587	3.3V_AUX
588	3.3V_AUX	589	3.3V_AUX
590	3.3V_AUX	591	3.3V_AUX
592	3.3V_AUX	593	3.3V_AUX
594	3.3V_AUX	595	3.3V_AUX
596	3.3V_AUX	597	3.3V_AUX
598	3.3V_AUX	599	3.3V_AUX
600	3.3V_AUX	601	3.3V_AUX
602	3.3V_AUX	603	3.3V_AUX
604	3.3V_AUX	605	3.3V_AUX
606	3.3V_AUX	607	3.3V_AUX
608	3.3V_AUX	609	3.3V_AUX
610	3.3V_AUX	611	3.3V_AUX
612	3.3V_AUX	613	3.3V_AUX
614	3.3V_AUX	615	3.3V_AUX
616	3.3V_AUX	617	3.3V_AUX
618	3.3V_AUX	619	3.3V_AUX
620	3.3V_AUX	621	3.3V_AUX
622	3.3V_AUX	623	3.3V_AUX
624	3.3V_AUX	625	3.3V_AUX
626	3.3V_AUX	627	3.3V_AUX
628	3.3V_AUX	629	3.3V_AUX
630	3.3V_AUX	631	3.3V_AUX
632	3.3V_AUX	633	3.3V_AUX
634	3.3V_AUX	635	3.3V_AUX
636	3.3V_AUX	637	3.3V_AUX
638	3.3V_AUX	639	3.3V_AUX
640	3.3V_AUX	641	3.3V_AUX
642	3.3V_AUX	643	3.3V_AUX

Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



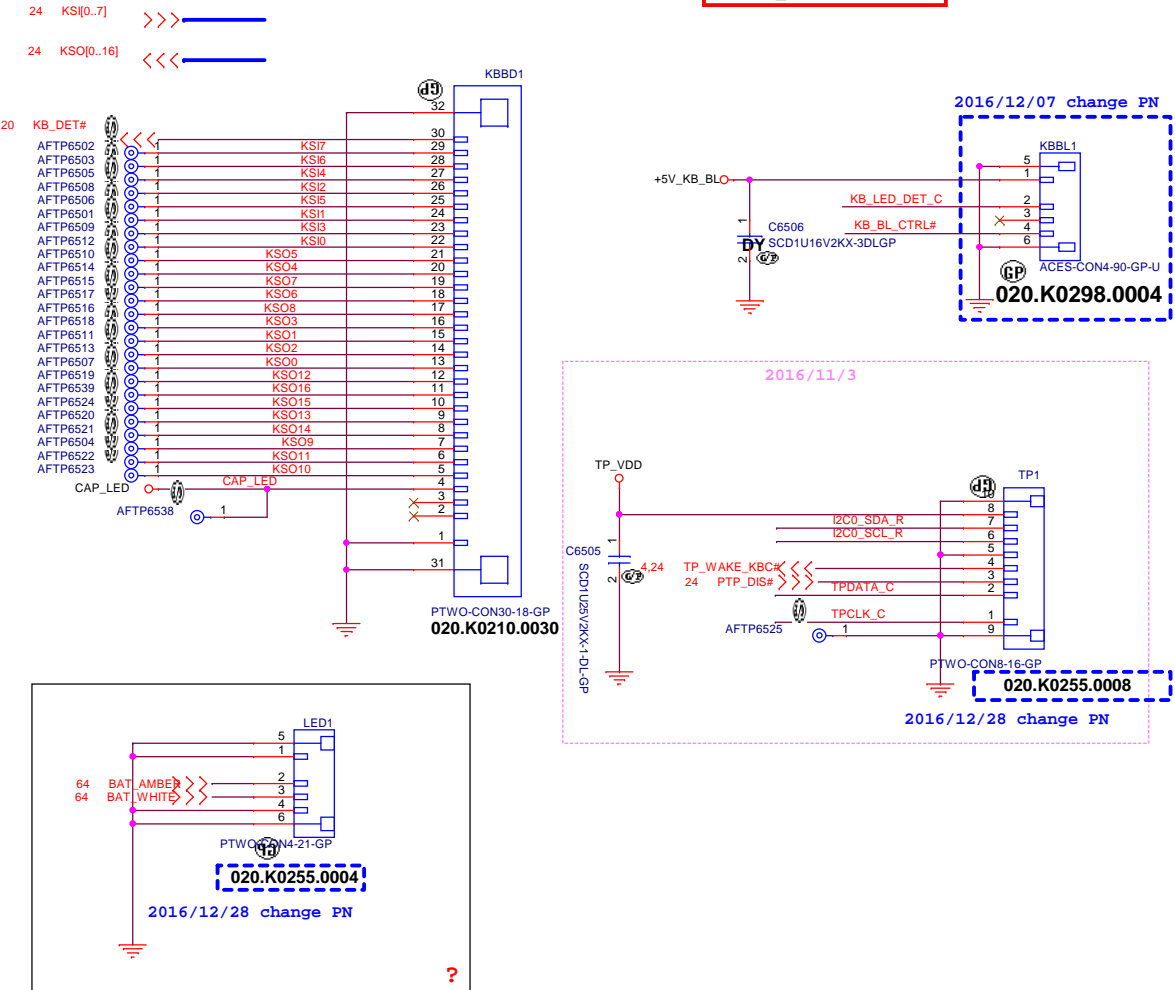
Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

SATA LED

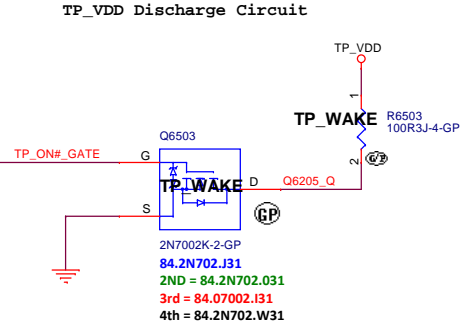
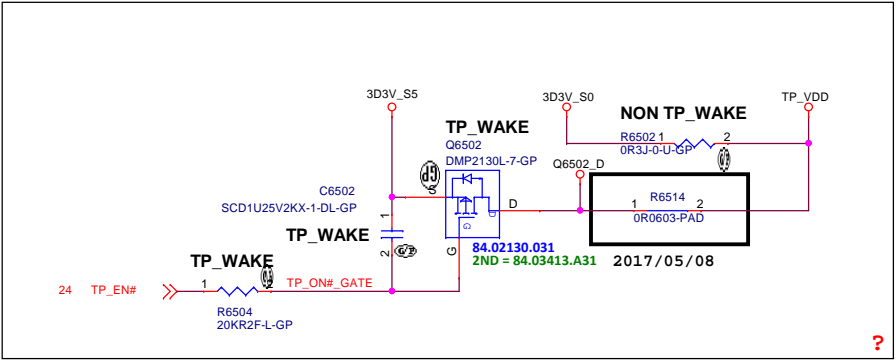


SSID = KB

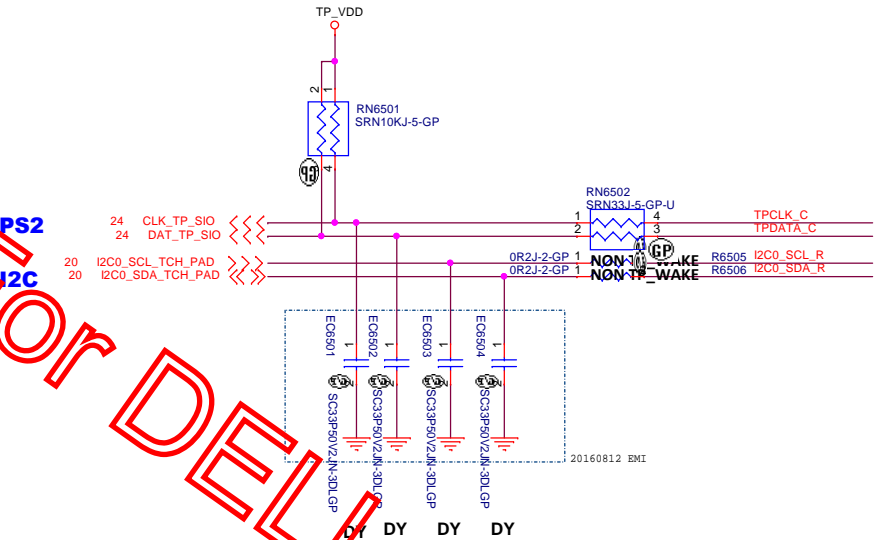
Keyboard



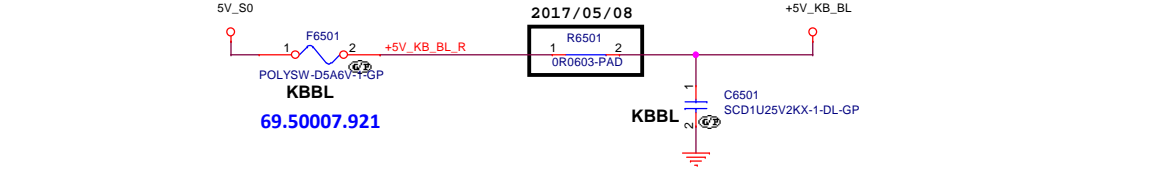
SSID = TPAD



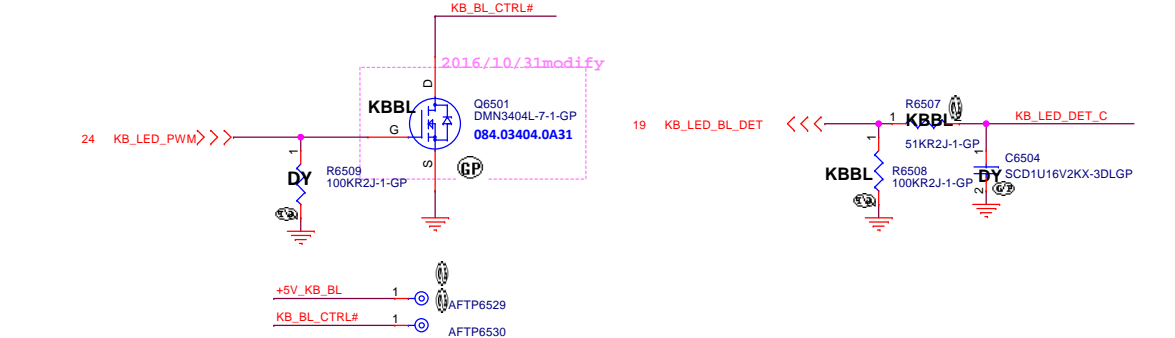
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



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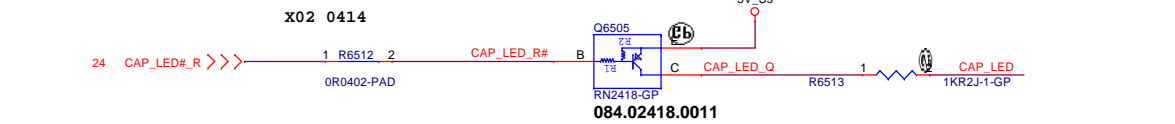


KB Backlight Power Consumption: 285mA max.

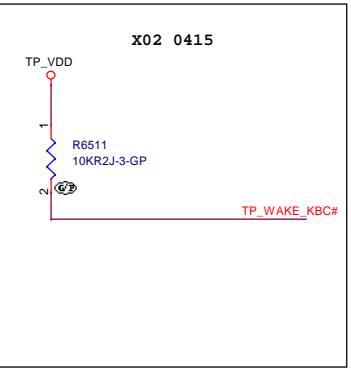


CAP LED Control

LOW activated from KBC GPIO



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

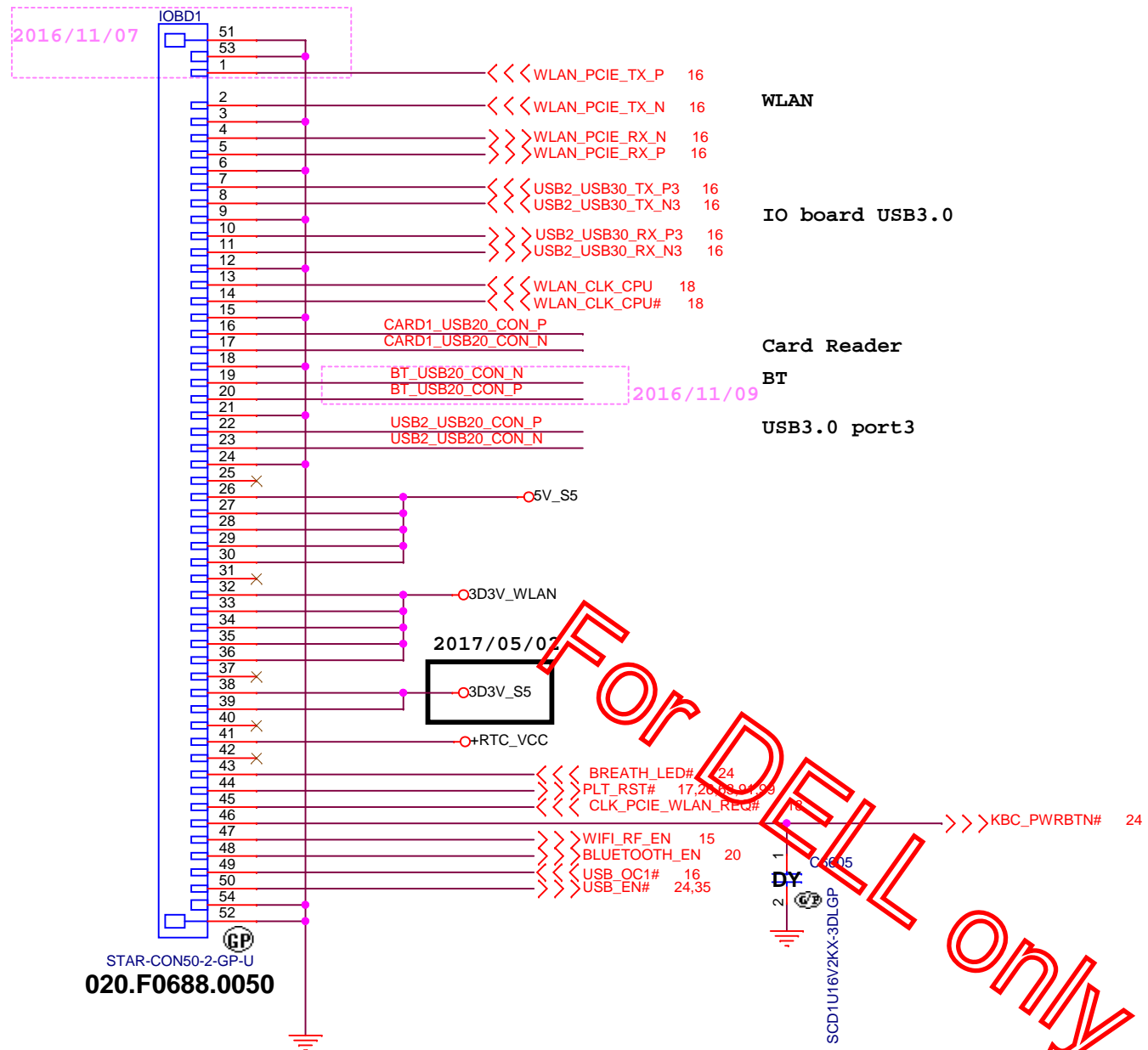


Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



<Core Design>

SSID = IO Connector



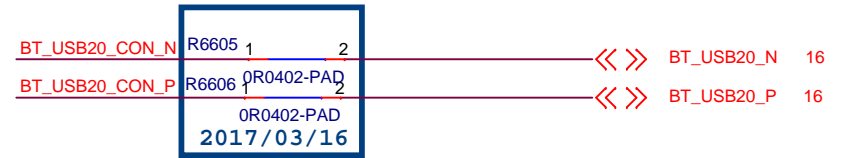
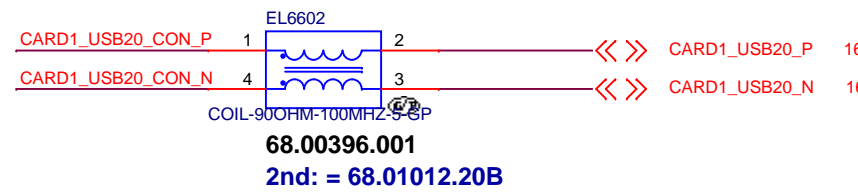
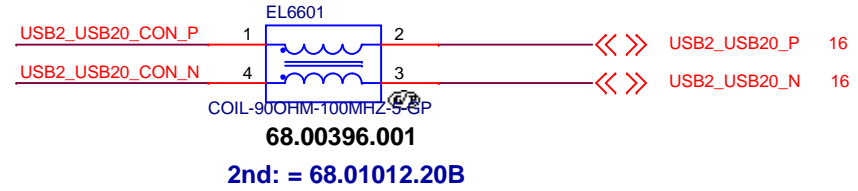
CARD1_USB20_CON_P	1	AFTP6601
CARD1_USB20_CON_N	1	AFTP6602
BT_USB20_CON_P	1	AFTP6603
BT_USB20_CON_N	1	AFTP6604
USB2_USB20_CON_P	1	AFTP6605
USB2_USB20_CON_N	1	AFTP6606
3D3V_S5	1	AFTP6607
5V_S5	1	AFTP6608

2016/12/07 add AFTP

KBC_PWRBTN#	1	AFTP6609
-------------	---	----------

2016/12/16 add AFTP

Change choke Height just for Starload
2015/09/23 modify



<Core Design>



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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

(Blanking)

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<Core Design>



Wistron Corporation

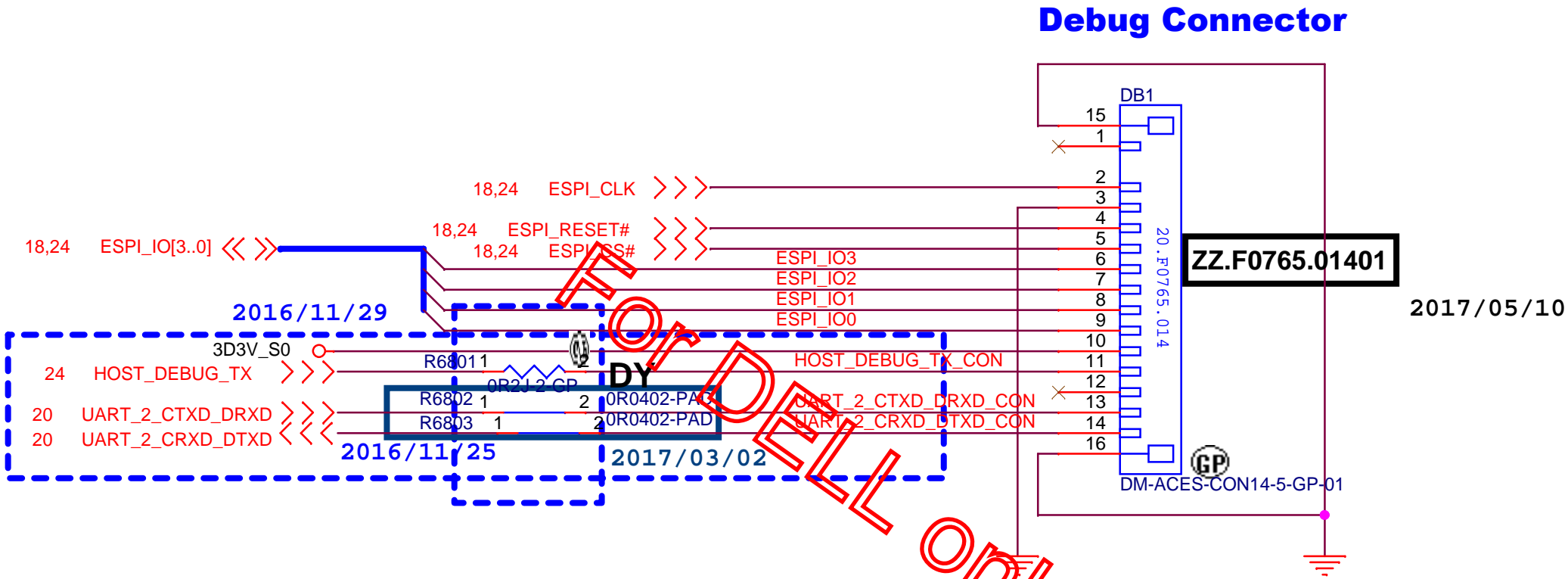
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size A4	Document Number <i>KyloRen 13"</i>	Rev <i>A00</i>
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SSID = Debug



Use ZZ.F0765.01401 DUMMY PAD for MP


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number KyloRen 13"		Rev A00
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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

(Blanking)
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<Core Design>



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SSID = Hall Sensor



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- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602




- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)
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<Core Design>



Wistron Corporation

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Title


RESERVED

Size A4	Document Number KyloRen 13"	Rev A00
Date: Thursday, June 29, 2017	Sheet 71 of	106

5	4	3	2	1
D				D
C				C
B				B
A				A

(Blanking)
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<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>USB3.0 PORT</i>			
Size A4	Document Number <i>KyloRen 13"</i>		Rev <i>A00</i>
Date: Thursday, June 29, 2017	Sheet 72	of	106

Main Func = dGPU

(Blanking)

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU(1/5)PEG			
Size A4	Document Number KyloRen 13"		Rev A00
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Main Func = dGPU

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Main Func = dGPU

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Main Func = dGPU

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<Core Design>



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Title

GPU(5/5)PWR/GND

Size

Custom

Document Number

KyloRen 13"

Rev

A00

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SSID = VRAM

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Title

GPU-VRAM1,2 (1/4)

Size

Document Number

KyloRen 13"

IV	
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Sheet 78

6

SSID = VRAM

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Main Func = dGPU

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<Core Design>

		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title GPU(5/5)PWR/GND			
Size Custom	Document Number KyloRen 13"		Rev A00
Date: Thursday, June 29, 2017	Sheet 80	of	106

Main Func = dGPU

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM1,2 (1/4)			
Size	Document Number		Rev
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Main Func = dGFX_CORE


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Main Func = dGPU

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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM7,8 (4/4)					
Size	Document Number				Rev
A3	KyloRen 13"				A00
Date:	Thursday, June 29, 2017			Sheet	84 of 106

Main Func = dGFX_CORE

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<Core Design>

		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title GPU CORE			
Size A2	Document Number KyloRen 13"		Rev A00
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Main Func = dGPU

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<Core Design>

		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title GPU Discrete Power			
Size A2	Document Number KyloRen 13"		Rev A00
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(Blanking)

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<Core Design>



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Title

Size
A3

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KyloRen 13"


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<Core Design>



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Title

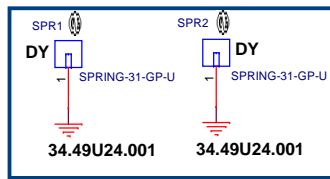
Reserved

Size A3	Document Number KyloRen 13"	Rev A00
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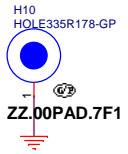
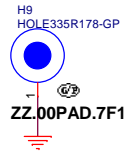
SSID = Unused Parts

34.4YW18.001



2017/03/21

ZZ.00PAD.7F1



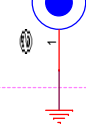
Type-C

2016/11/7modify

34.4SE26.201

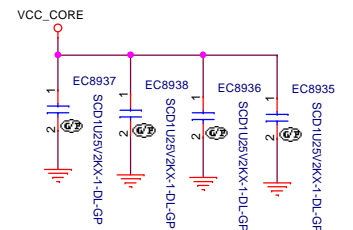
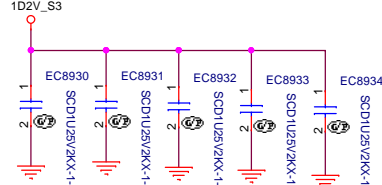
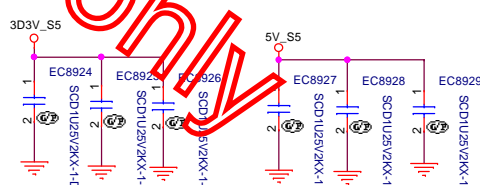
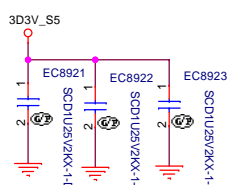
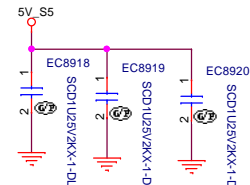
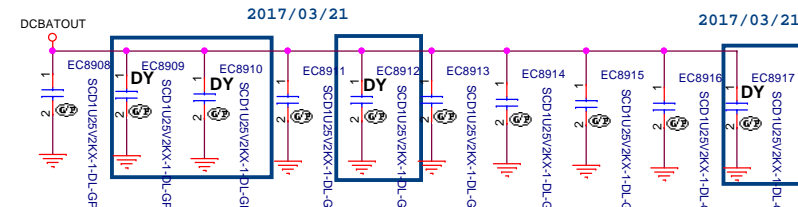
HS1

STF237R113H62-10-GP

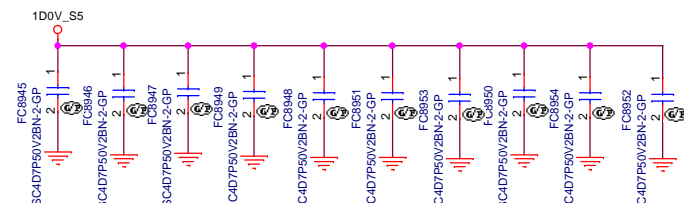
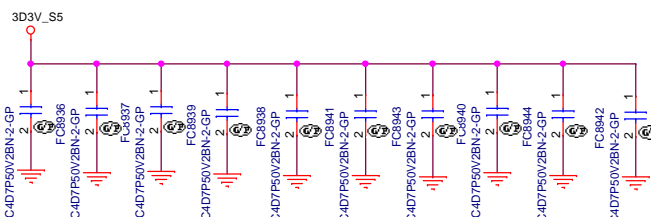
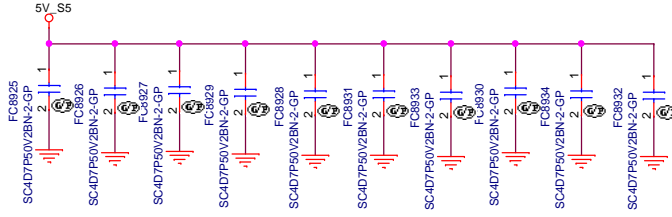
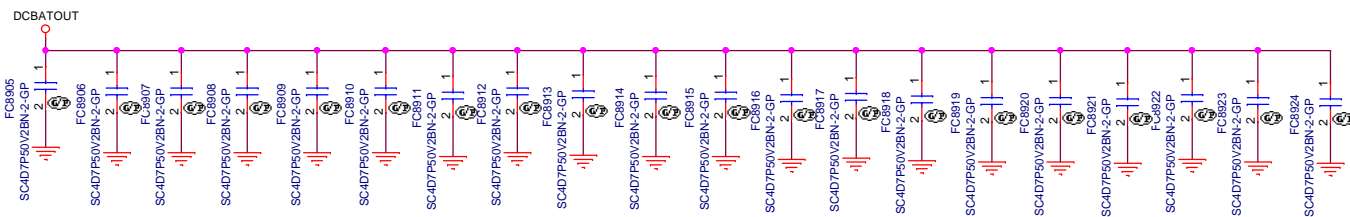


SSID = EMI

Mind the voltage rating of the caps.



SSID = RF



<Core Design>

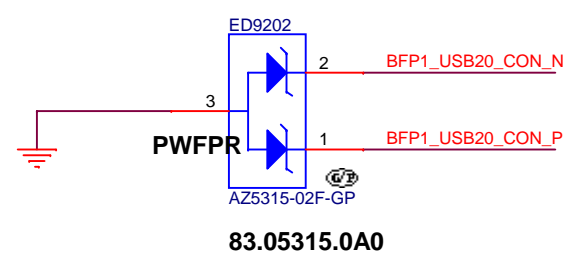
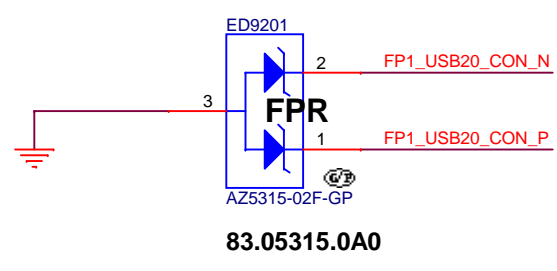
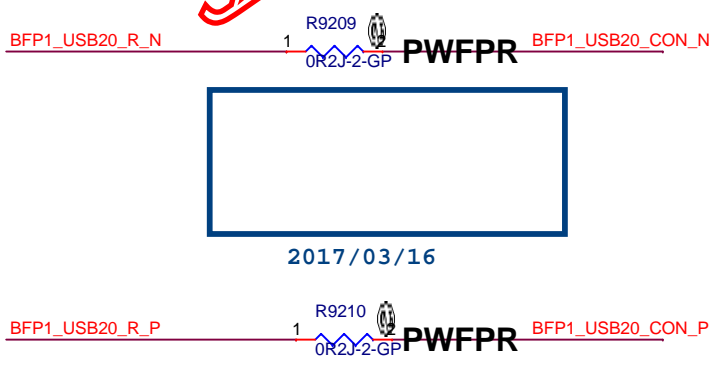
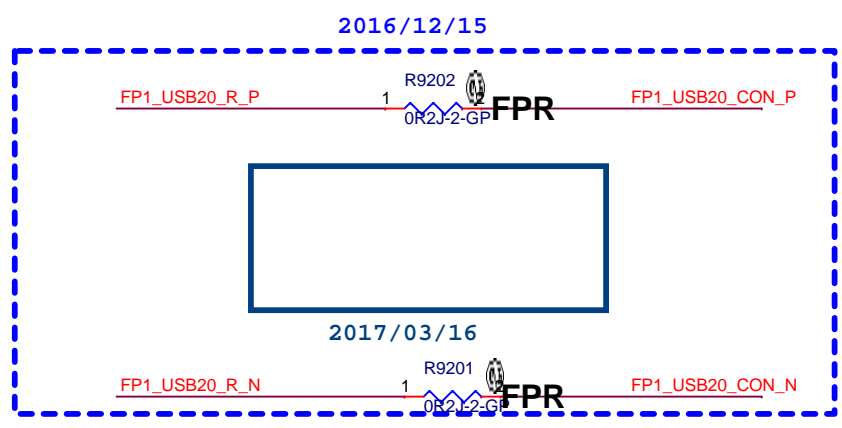
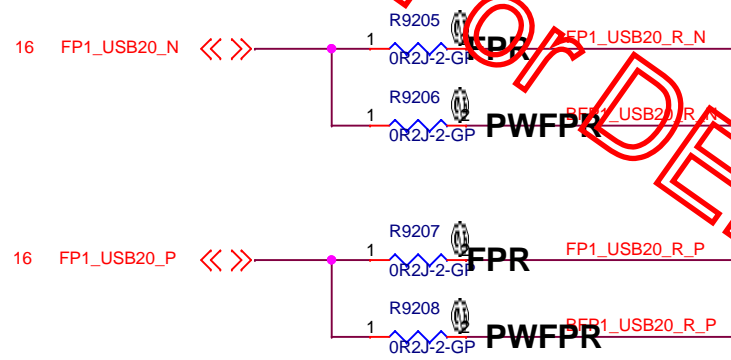
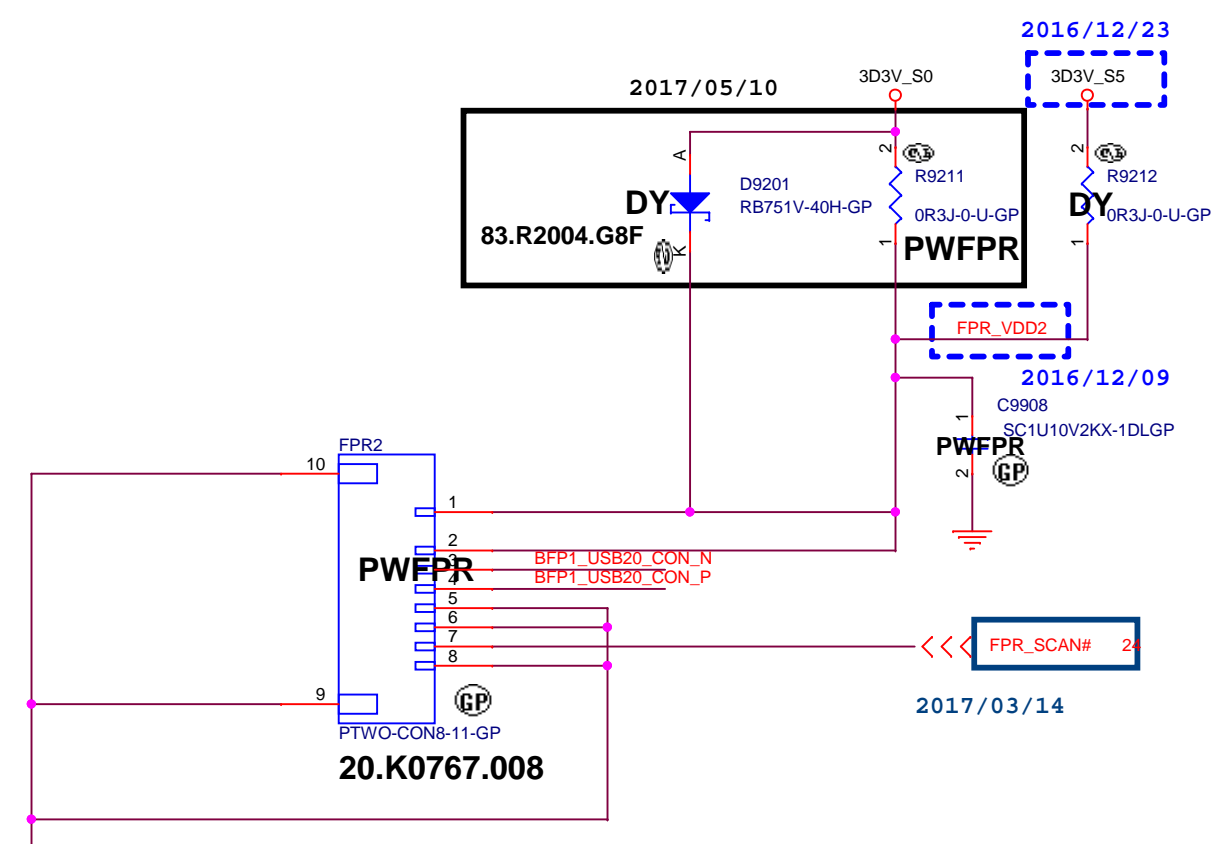
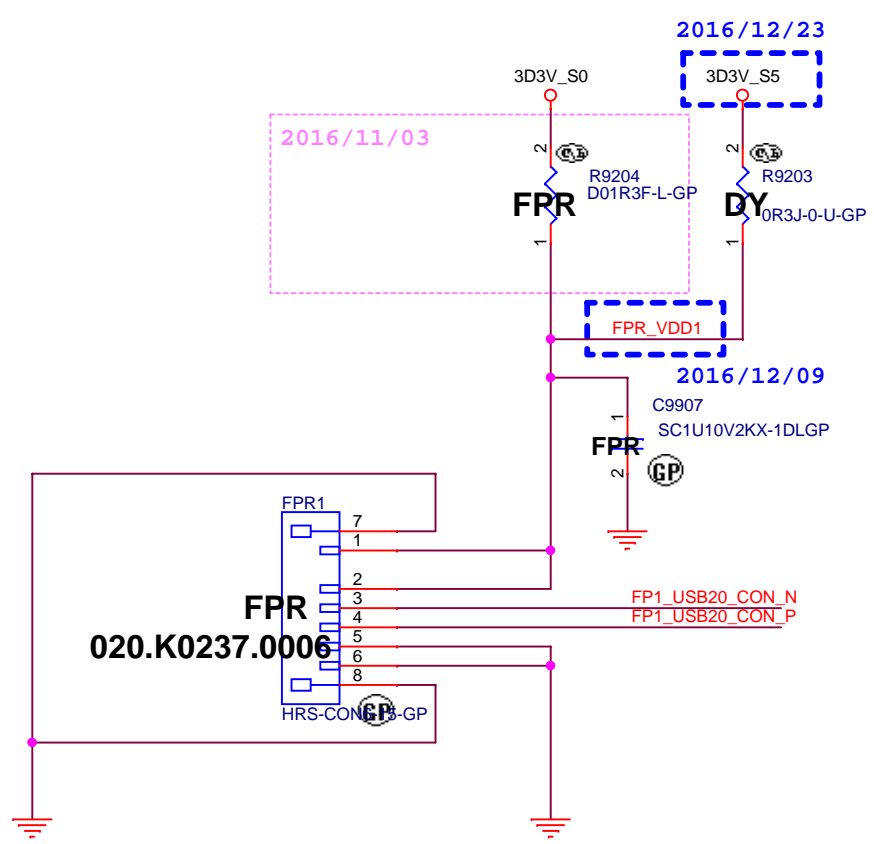
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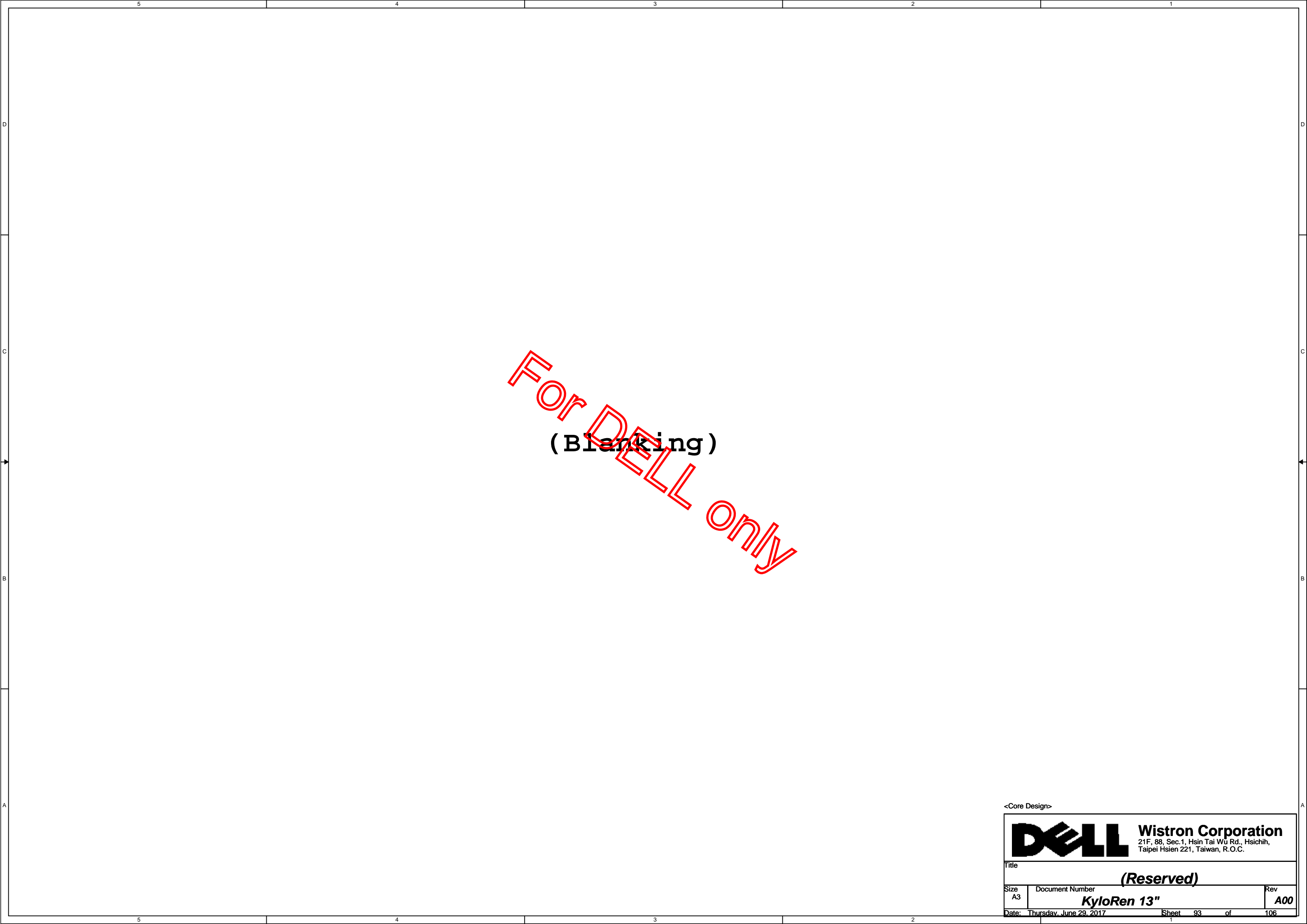
For DELL only

SSID = FPR

FBR(finger Print Sensor)

FBR(Botton side finger Print Sensor)






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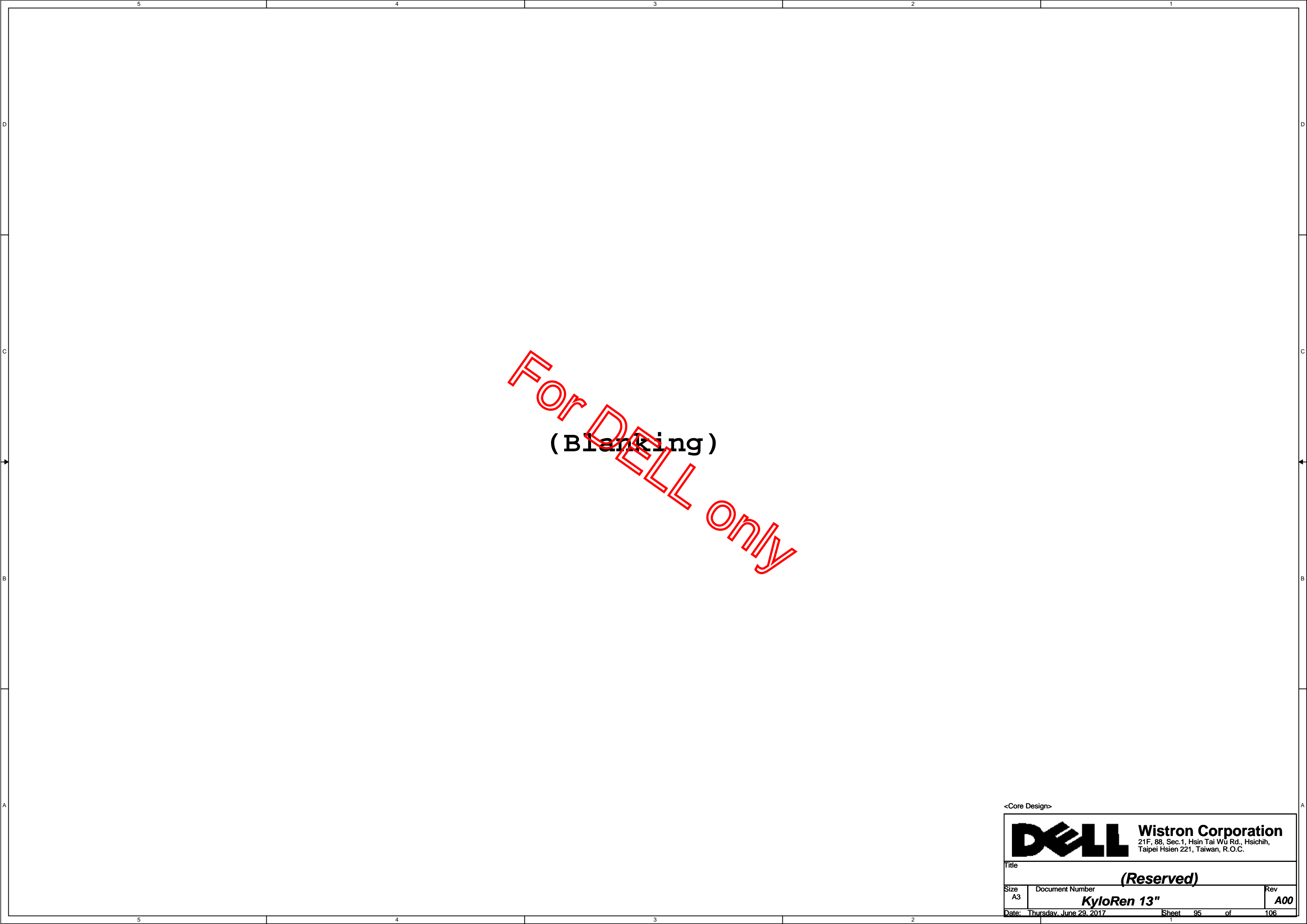
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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
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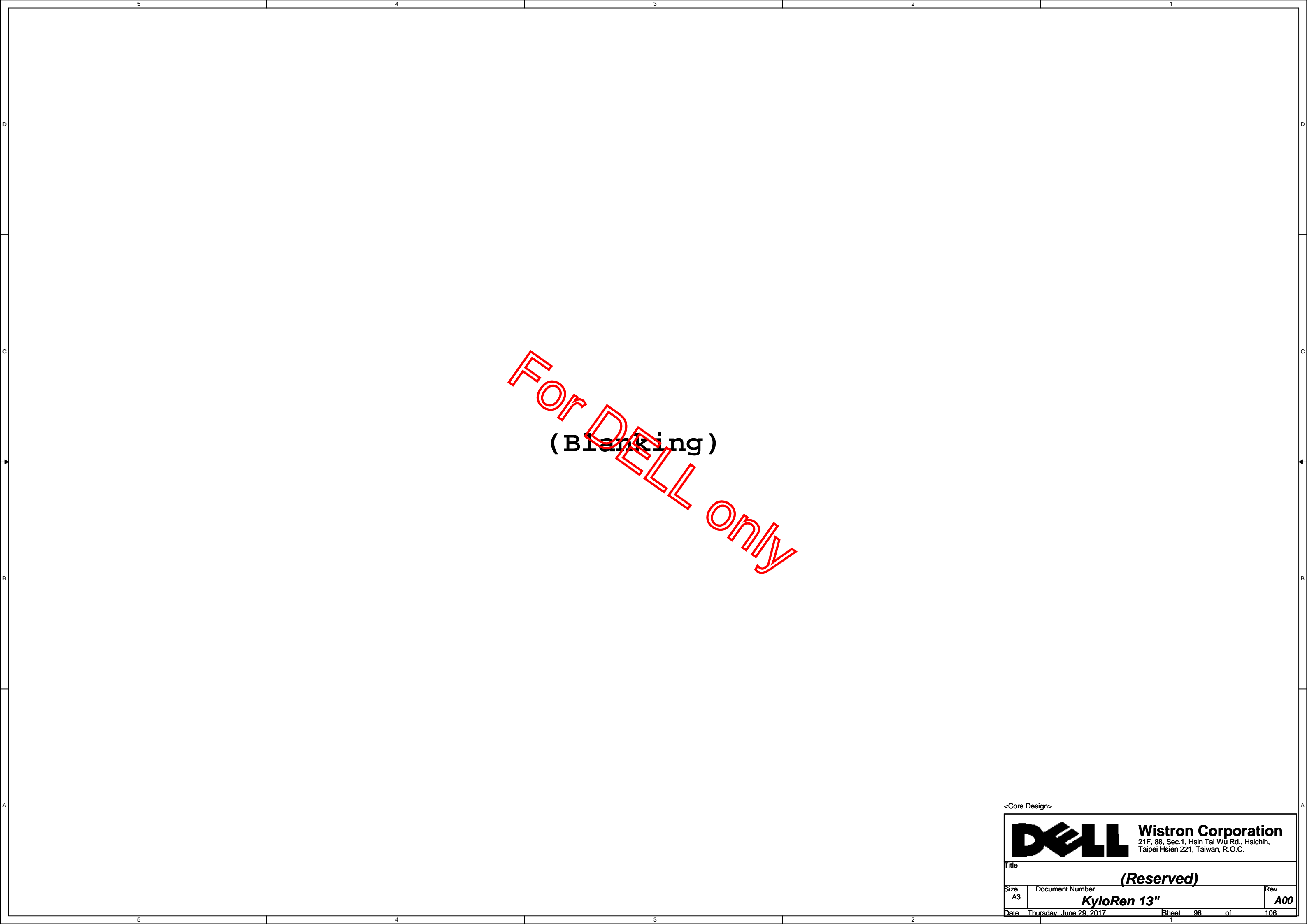


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(Reserved)					
Size	Document Number				Rev
A3	KyloRen 13"				A00
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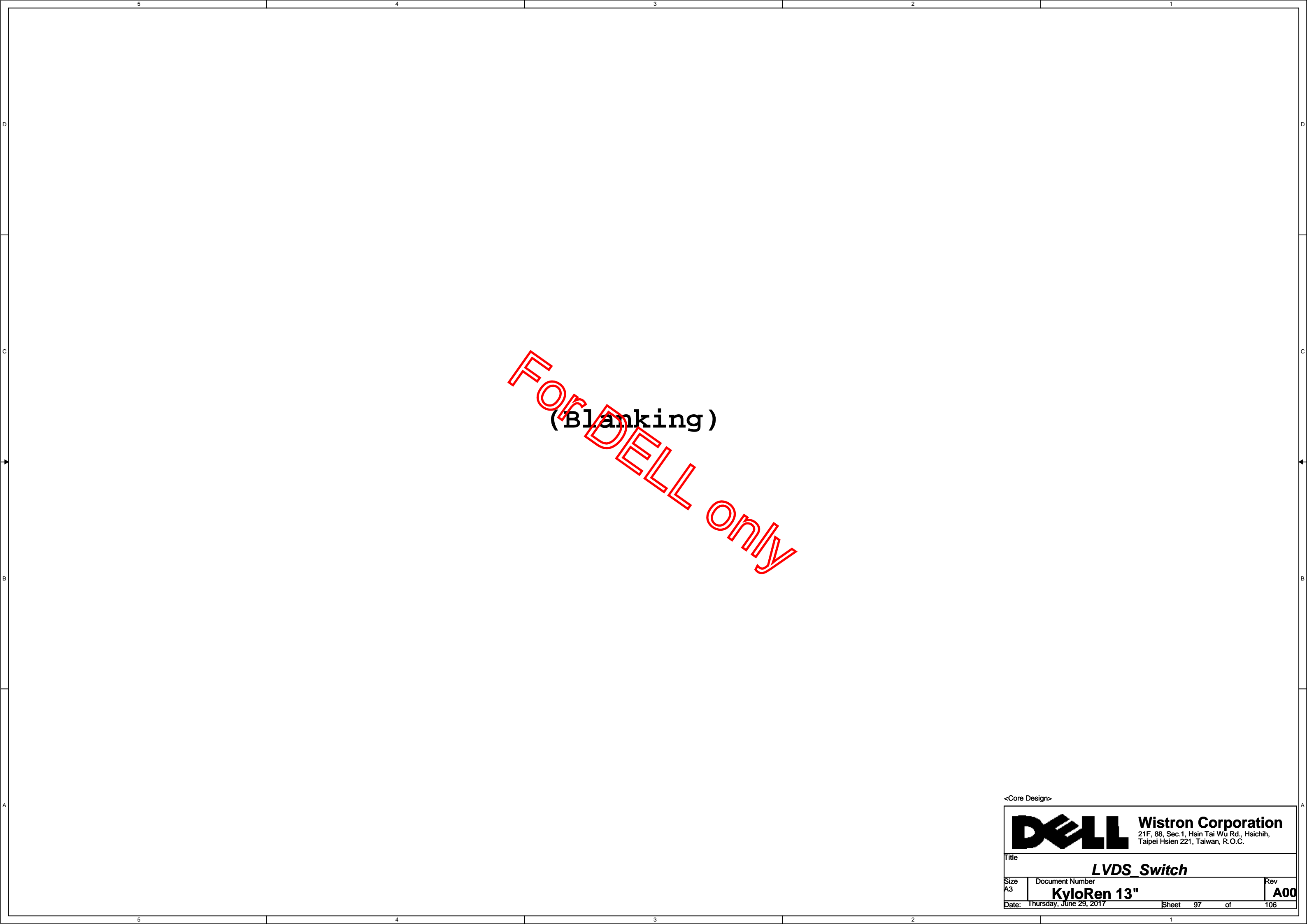


<Core Design>



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Title		
(Reserved)		
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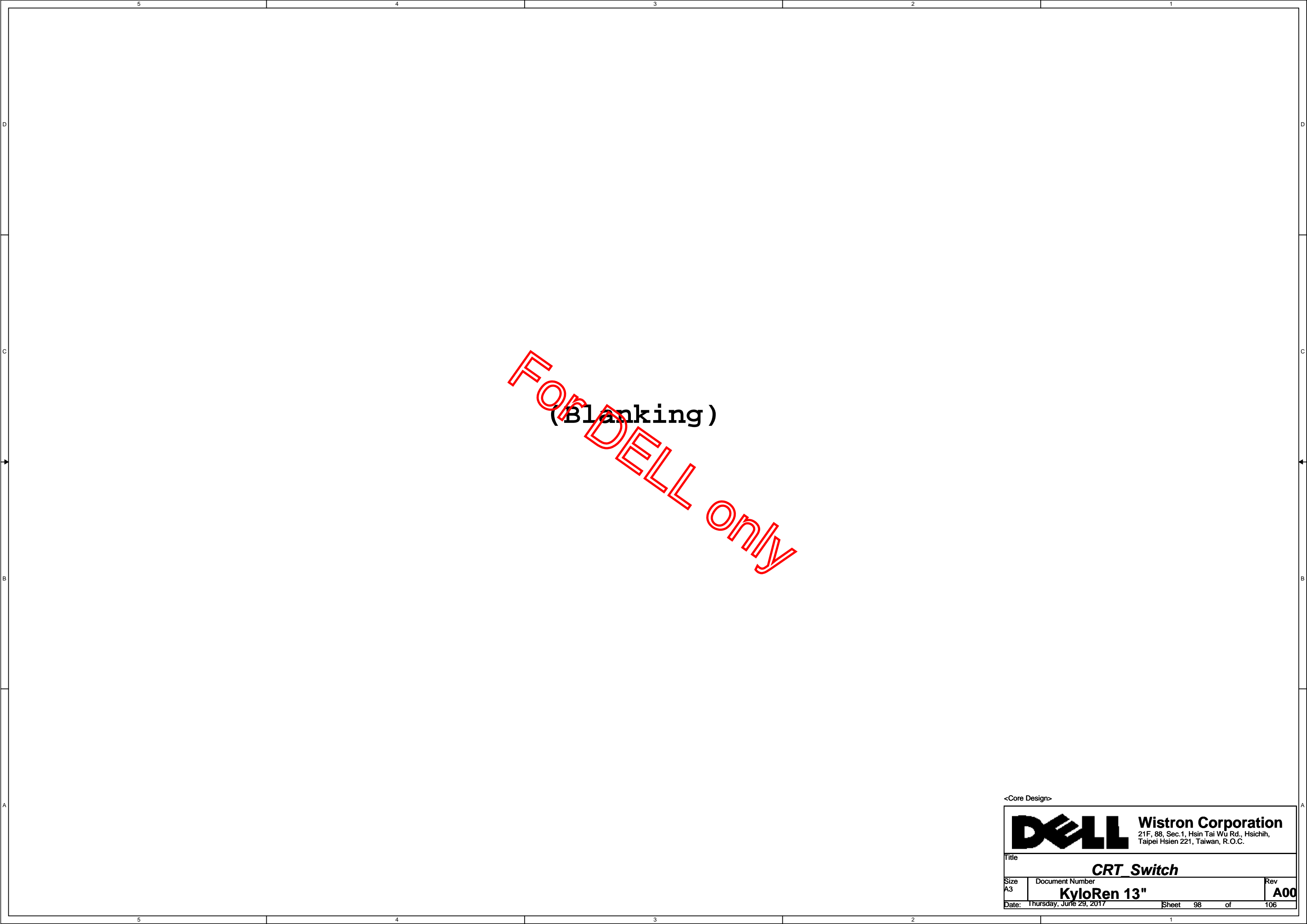


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Title			
LVDS Switch			
Size A3	Document Number KyloRen 13"		Rev A00
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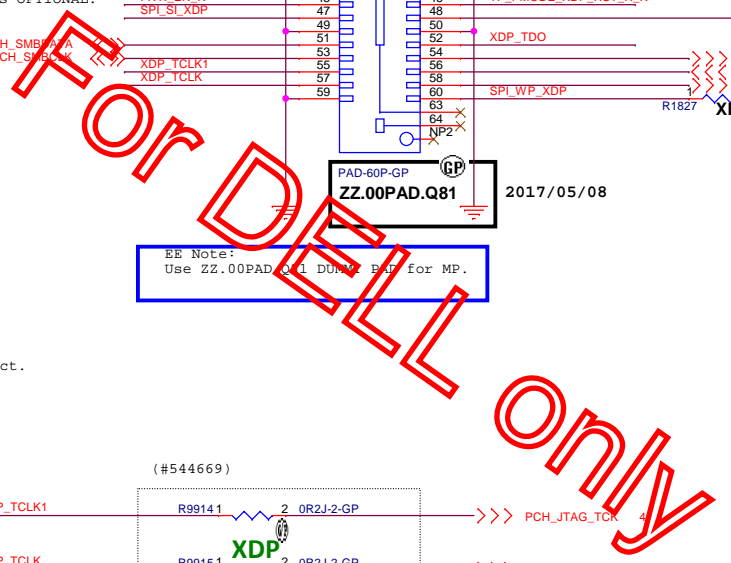


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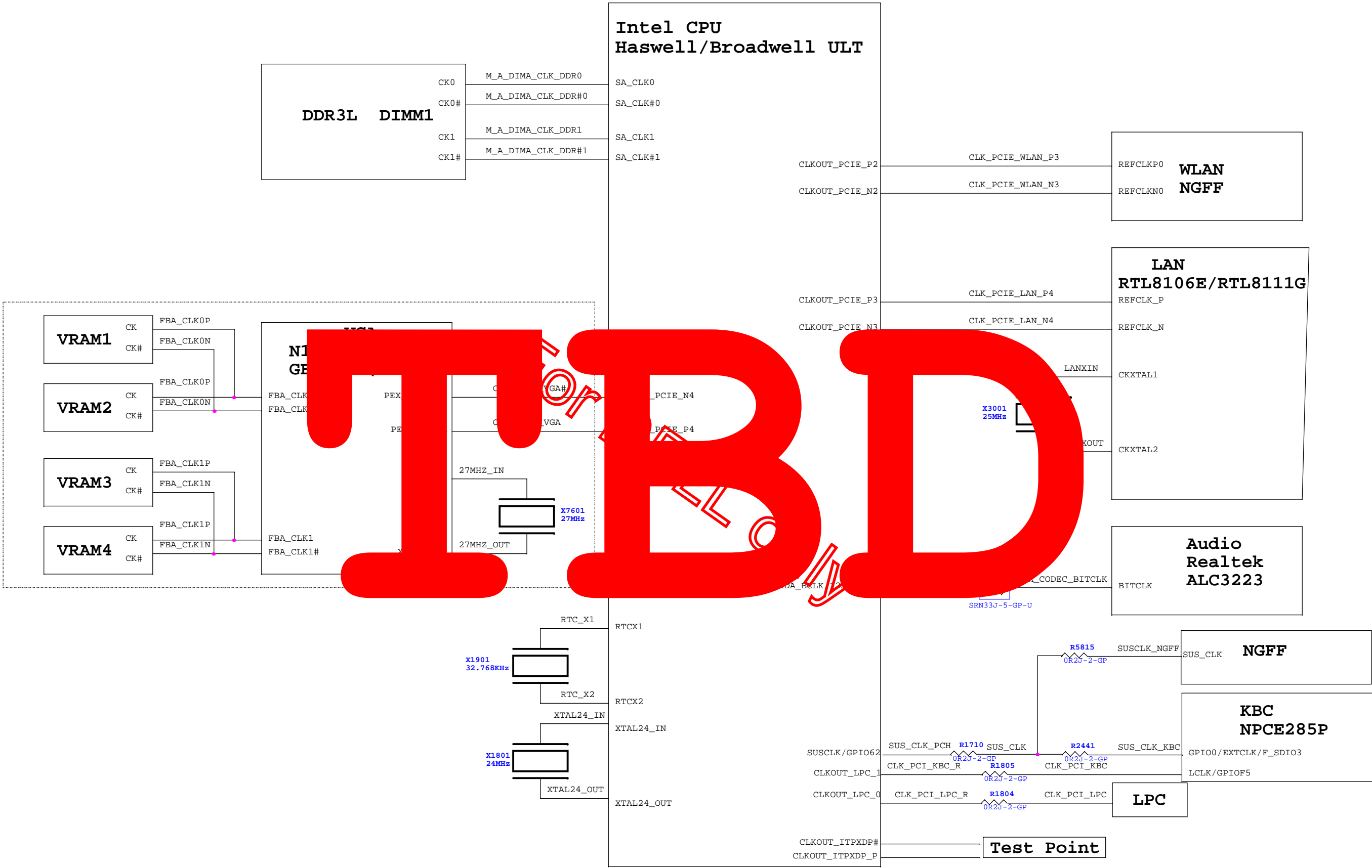
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<div><div>DELL</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>CRT Switch</div>		
Size <div>A3</div>	Document Number <div>KyloRen 13"</div>	Rev <div>A00</div>
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This signal has a weak internal pull-up.

CLK Block Diagram



[illegible]

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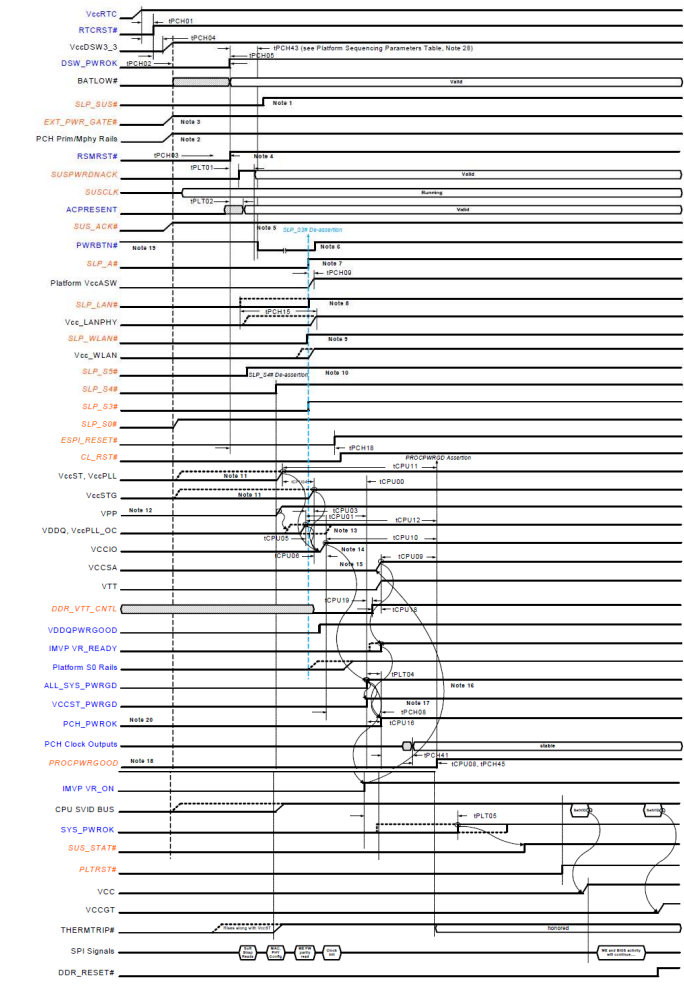
	Title
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Change History		
Size	Document Number	Rev

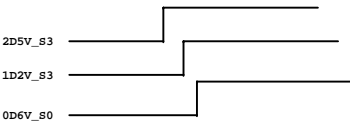
Size A3	Document Number KyloRen 13"	Rev A00
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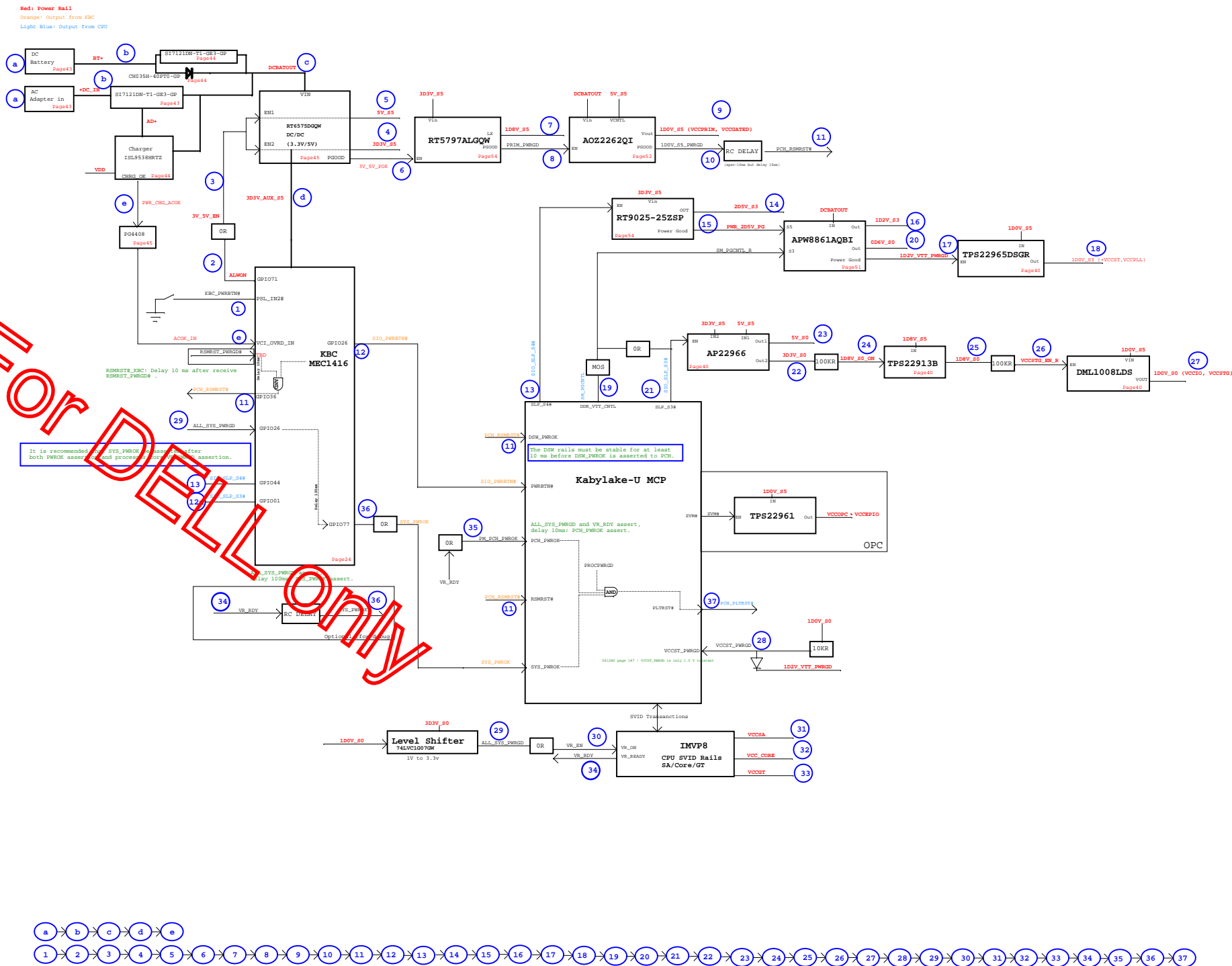
SKL-UY Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

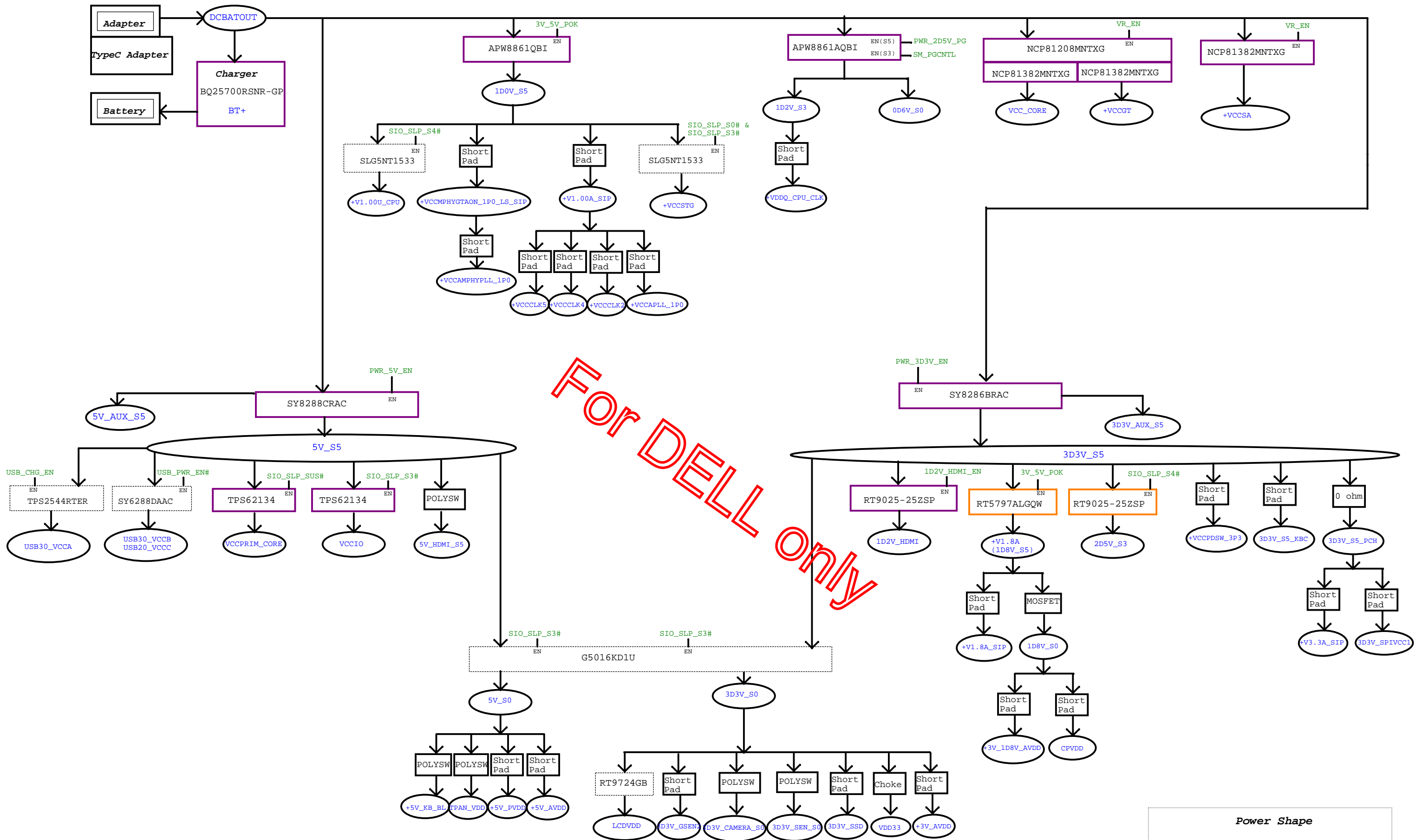


For DDR4 power sequence



Kabylake POWER UP SEQUENCE DIAGRAM (Non-Deep Sx Platform)





Power Shape

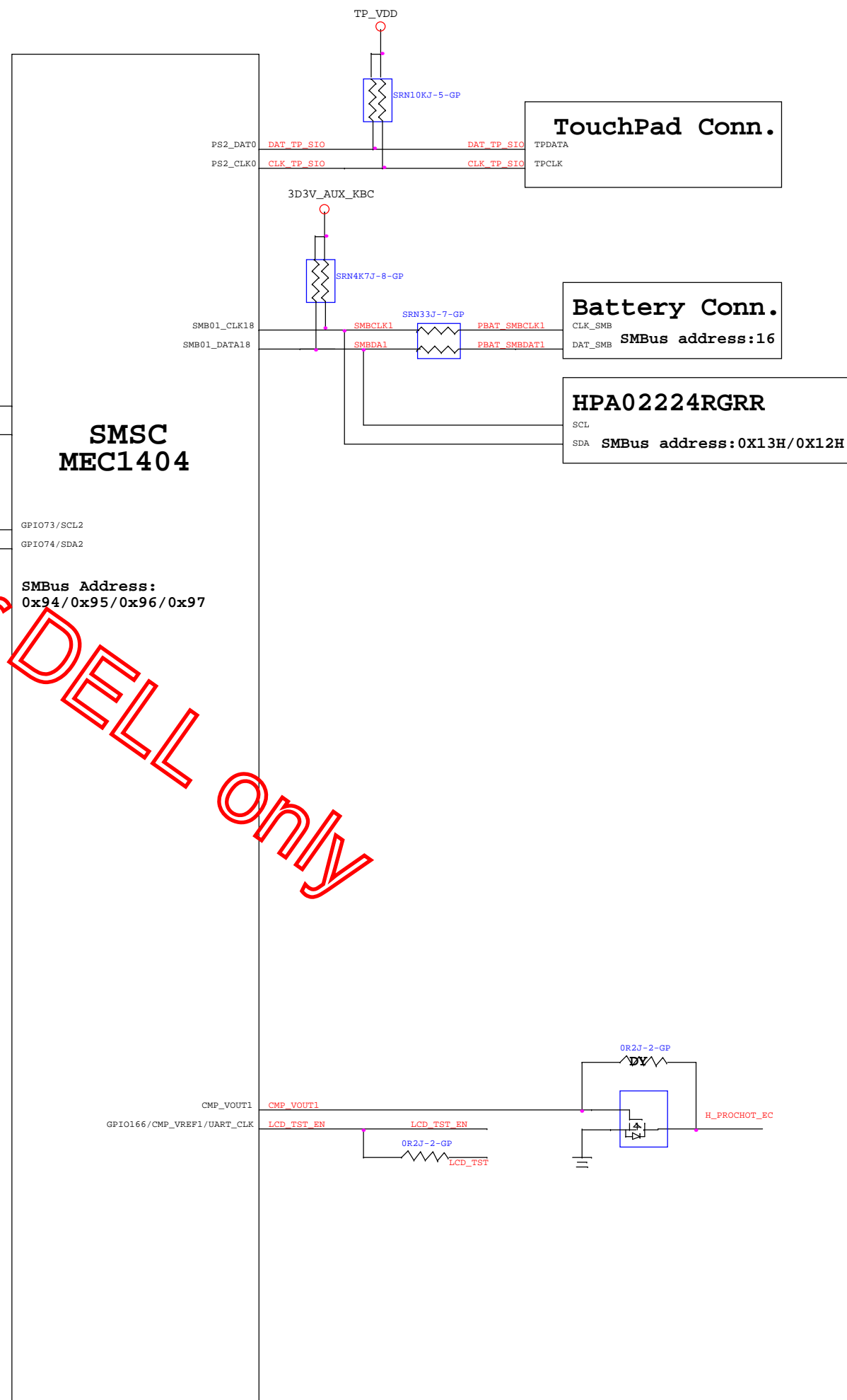
Regulator

LDO

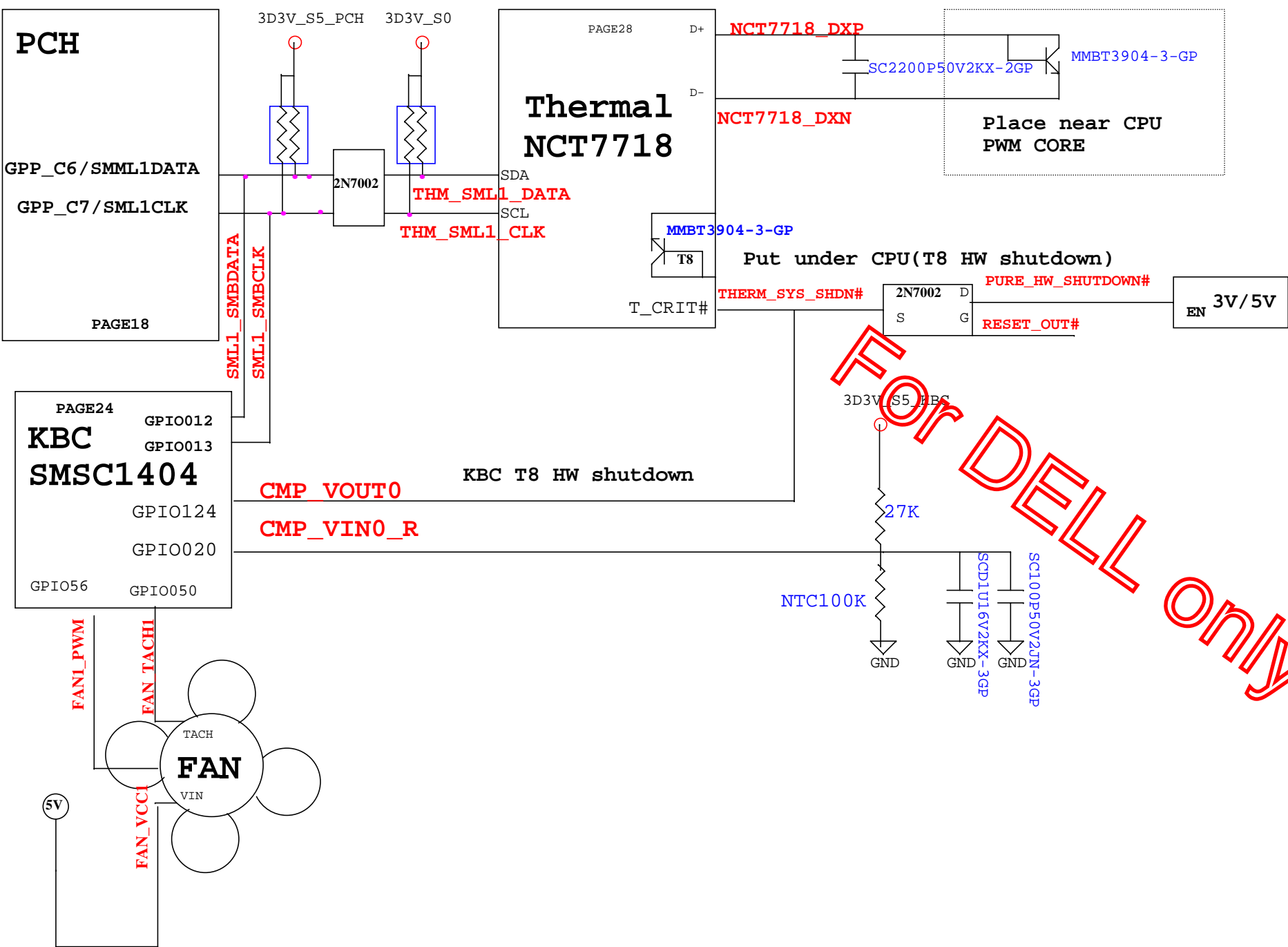
Switch

<Core Design>

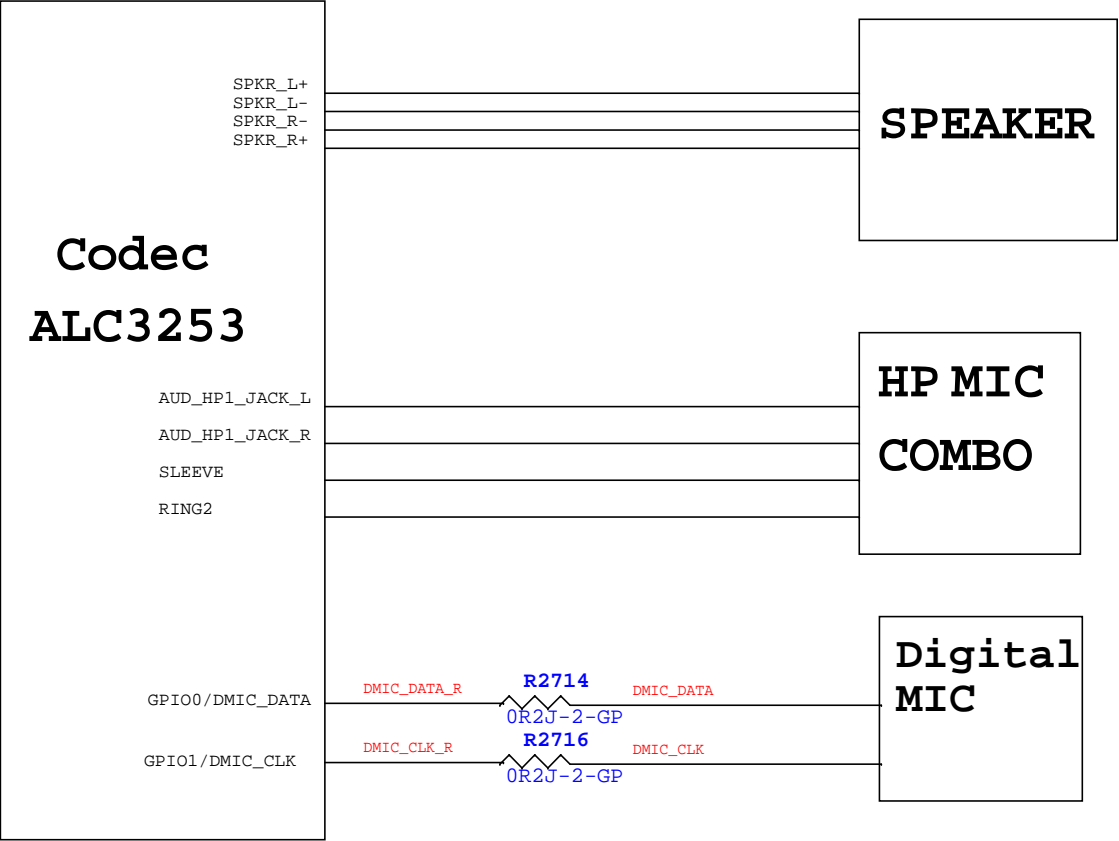
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>




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